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# An Approach for Logic design perspective of Metastability

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## Abstract

Metastability is a phenomenon that can cause system failures in digital circuits. It may occur whenever signals are being transmitted across asynchronous or unrelated clock domains. This paper defines what metastability is, ways of interpreting it, ways of predicting metastability the issues concerning it and ways to limit metastability also the remedies suggested. Ways to limit Metastability include only one clock, using faster flip flops decreasing the asynchronous input frequency and using synchronization hardware. I have tried to provide the logic design perspective of metastability rather than the circuit level design view. I have mentioned all the references that I have gone through.

***Keywords**: MTBF, Synchronizer*

## I. Introduction

Reliability is important to understand metastability operation of flip-flops. To achieve high reliability careful device evaluation characteristics or good synchronous design should be in practice. Reliability is extremely important to digital circuit designers. To ensure reliability certain timing requirements of flip-flop have to be met. Thus if these requirements are violated, metastable outputs occur. Metastable outputs are not logic high or logic low and can cause delays and system failures. Research and recognition of metastablity occurs in early 1970's and continues today. The importance of metastability is without question. For certain minimal timing requirements of ensuring good logic 0 and logic 1, above condition have to be met by sequential components for the data arrival.

The data should arrive a minimum time before the active edge of the clock (and remain stable) for the clock to latch. Destination register is violated; the output of the register has a chance to become metastable, a condition where the output voltage is neither high nor low. But however at some intermediate voltage for an indefinite period of time eventually, the metastable value will resolve to a state of logic-**0** or logic-**1**.

Designers often use back to back flip-flops, called synchronizer chain to reduce the chance of metastable events propagating through the design. An example of synchronizer is shown in fig.1 (b). From the fig. each flip-flop in the except the last, feeds only one flip-flop so there is no chance of a metastable output being resolved Differently by two fan-out flip-flops and the failure mechanism of Fig.1 (a) does not occur within the chain.

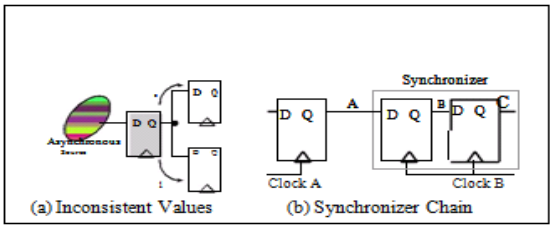


*Fig.1 Metastablity propagation*

Once the flip-flop has entered the metastable state, the probability that it will still be metastable sometime later has been shown to be an exponentially decreasing function as in fig.2.

The designers need to know the characteristics of metastability so that he can determine how long he must wait to achieve his design goals.

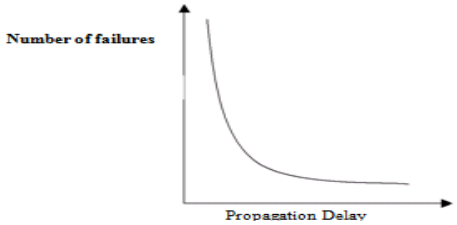


*Fig.2. Number of failures v/s Propagation delay*

## II. What is Metastability?

Metastablity is potential catastrophic event that occur when asynchronous inputs and flip-flop are used. Metastability in digital system occurs when two asynchronous signal combine in such a way that their resulting output goes to an intermediate state. A common example is the case of data violating setup and hold specification of a latch or a flip-flop. The data should arrive a minimum time before the active edge of the clock (and remain stable) for the clock to latch a valid logic of the data (setup time) and similarly this data should also remain stable for a minimum specified time after the active edge of the clock (hold time). Whenever there is any violation, the output voltage is anywhere

between a logic high and a logic zero. In such a condition the flip-flops takes additional time to settle to astable output. There is no way that the final state can be predicted.

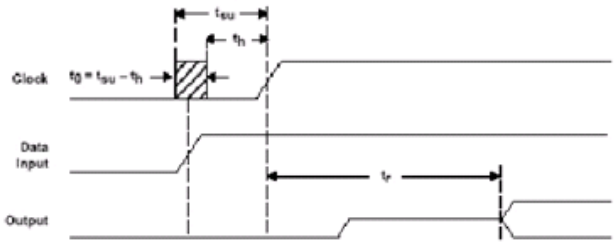


Fig.3 (1).*Timing diagram*

This operation is analogous to a ball rolling over a hill {Fig.3 (2)}.Each side of the hill represents a stable state and the top of the hill represents the metastable state. Whenever the flip-flops satisfies the setup and hold timings, the output achieves a stable state (either 1 or 0).

This is analogous to the ball at the top of the mountain in theory, since the flip-flop used is bistable device which means it will be only stable at logic high or logic zero, any instability will "roll" down towards one of these two states. The output will not stay in metastable state, just as a ball will not stay on top of the hill.

*Fig* 3(2).*Ball rolling over hill*

When the output becomes metastable it will however between low and high states which is represented in Fig.4 after a certain amount Of time, the output unpredictably reverts to either low or high states.

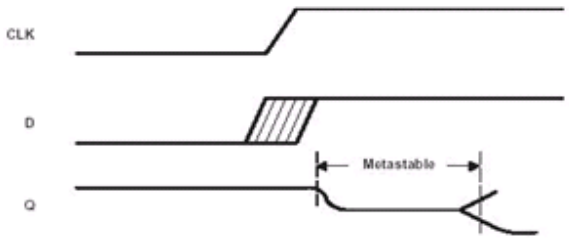


*Fig.4.Timing diagram of metastable state*

## III. Predicting Metastability

There are some cases where metastability occurs, as we have seen that whenever there is setup and hold time violation metastability occurs, so it is seen when the signal violates this timing requirements.

- When the clock skew is more (rise time and fall time is more than tolerable values
- When the input signal is asynchronous signal
- When interfacing two domains operating at two different frequency

Metastability can be described by mathematical equation no.1.It is about mean time between failures (MTBF). Different parameters that have to be taken into account include the frequency of the asynchronous input signal ($f_{in}$), the clock frequency ($f_{clk}$) and the time delay between the clock edge and a stable response on the output when metastability occurs ($t_x$).

$$MTBF = \frac{Exp\,(T * t_x)}{f_{clk} * f_{in} * t_o} \qquad (1)$$

The exponential term in the equation describes the probability that a metastable condition will last for time t.

## IV. Limiting Metastability

It is not possible completely to prevent the metastability; however design suggested should be able to limit the possibility of metastable behavior to a certain level of extent. Some of the ways to do this is to include one clock using faster flip-flop, decrease the asynchronous input frequency, and use synchronous hardware. This approach, while simple is rarely practical given the performance requirements of most modern designs.

The following few methods are used to avoid metastablity:

- Synchronize any asynchronous input through one path that has at least one and preferably two flip-flops in series. The flip-flops should be running on the same edge of your system clock as the rest of the circuit this will limit the area of potential problems to one path instead of several and minimize the possibility of metastability entering the main part of the circuit .use buffered flip-flops or unbuffered flip-flops with minimum load. The second flip-flop output will correct after two clocks, since the odds of two metastable events occurring back-to- back is almost nil. In a practical circuit, cascading two flip-flops and at reasonable data rates, errors occur millions or even billions of year apart. Good enough for most systems. But "correct" means the second stage's output will not be metastable: it's not oscillating, nor is it at an illegal voltage level. There is still a chance the value will be either legal logic state .Thus this is a very powerful technique.
- Compute a parity or checksum of the input data before the capture register. Latch that into the register as well. Have the code compute parity

and compare it to that read. If there's an error, do another read.

- Use metastability hardened Flip-flops.
- Design any state machines whose operation is affected by these "synchronized" signals to follow a gray code pattern between states controlled by these signals. Gray code is a counting scheme where only a single bit changes between numbers, as follows:

000
001
011
010
110
111
101
100

- Using faster flip-flop decreases the setup and hold times of the flip-flop, which in turn decreases the time window that the flip-flop is free from metastability.

Some designs will never have a metastability problem. It always stems from violating set-up or hold times, which in turn comes from either poor design or asynchronous inputs. By following these few precautions, the circuit will be resistant to the effects of metastability and more reliable.

## V. Conclusion

The metastability characteristics of a device depend upon the process technology used for its design and the environmental conditions. Digital circuit's designers must determine the metastability characteristics of their circuits in order to ensure reliability.

They have become increasingly prevalent at higher operating frequencies. Various semiconductor companies employ different methods to tackle the problems arising due to metastability, few of which have been discussed. No matter what method is used, these failures must be accounted for in the design of asynchronous digital circuits.

Ways of limiting metastability include using only one clock, using faster flip flops, and decrease the asynchronous input frequency, and use synchronization hardware.

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