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Lower-Area Lower-delay Data Comparison Circuitry Using Modified BWA Based Architecture

Gopika Nath. G[1], Hima Sara Jacob[2] and Reneesh C. Zacharia [3]

[1] ECE Department, Mangalam College of Engineering, Ettumanoor, Kerala, India

[2] ECE Department, Mangalam College of Engineering, Ettumanoor, Kerala, India

[3] ECE Department, Mangalam College of Engineering, Ettumanoor, Kerala, India

Abstract

In a computing system, incoming information needs to be compared with a piece of stored data to locate the matching entry, e.g., translation look-aside buffer matching and cache tag array lookup. Before compare with the incoming data, decode and correction should performed if the stored data is protected with ECC. The total access time increases by using decoding and correction step. BWA is designed for efficient hamming distance computation. BWA circuitry replaced using modified half adder (HAM) and modified XOR gate (XORM). XORM has 1 gate less than the conventional XOR gate of 5 gates (AND-OR-NOT implementation). HAM has 2 gates less than the conventional half adder. As the number of gates reduces, area is reduced. By using this XORM and HAM in BWA based encoder circuitry, delay also reduced than conventional circuitry.

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1. Introduction

In a computing system, data comparison circuit has many applications. To enhance the reliability and data integrity of the memory structures, error correcting codes (ECC) are widely used in modern microprocessors. For example, modern rnicroprocessors caches are protected by ECC. A piece of data is encoded first and the entire codeword including the ECC check bits are written into the memory array, if a memory structure is protected with ECC. The loaded codeword should be decoded and corrected if errors are detected to obtain the original data.The result of the comparison determines the flow of the succeeding operations hence data comparison circuit is usually in the critical path of a pipeline stage.The cache tag directory must be accessed first in the cache tag match example. Before the comparison operation, the tag information must go through ECC decoding and correction. So the corresponding data array is waiting for the comparison result to decide which way set to load the data from[2].

An architecture is proposed for the removal of ECC decoding/correction from the critical path. Here, instead of decoding the coded word prior to the comparison, retrieved codeword is directly compared with the incoming information which is encoded. Complex decoding is eliminated from the critical path by using this direct compare method. For the Hamming distance computation, saturate adder (SA) is used[2].

For the faster hamming distance computation, proposes a low-complexity processing element. Here, both the tag comparison and the encoding process to generate the parity bits from the incoming tag are performed in parallel. Therefore the overall latency is reduced than SA based architecture. Here multiple butterfly-formed weight accumulators (BWAs) are used for improving the latency and complexity of the Hamming distance computation[1].

2. Previous Works

The conventional decoder and compare architecture, SA based encoder architecture and BWA (Butterfly Weight Accumulator) based encoder architecture are explained in this section.

2.1 Decoder and Compare Design

Before comparing with the tag field of the incoming address the encoded data go through ECC Decoders and ECC Correction logic. The sum of the tag directory access, time to decode and correct if necessary, the time needed for tag comparison and the time needed to select the matched way of the data array gives the total cache access time. A “cache miss” will occur if the incoming address does not match to any of the stored tags. The “ECC Gen” logic encodes the incoming tag and used to replace a way in the set just referenced. While, the

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corresponding data array is waiting for the comparison result to decide which way in the set to load the data from.

2.2 SA BASED ENCODER DESIGN

The encoded incoming tag field of the address is directly compared with the information retrieved from the tag directory. Note that the encoding of the incoming tag can be done in parallel with the tag directory access. Thus, the sum of the tag directory access time and tag comparison gives the total access time. From the access time the decoding and correction time has been removed. In both fig.1 and fig.2, the MCA signal refers to the Machine Check Architecture. In this the microprocessor has detected an uncorrectable error thus, the system requires to take action. The complexity and delay reduced by this design approach than decoder and compare method.

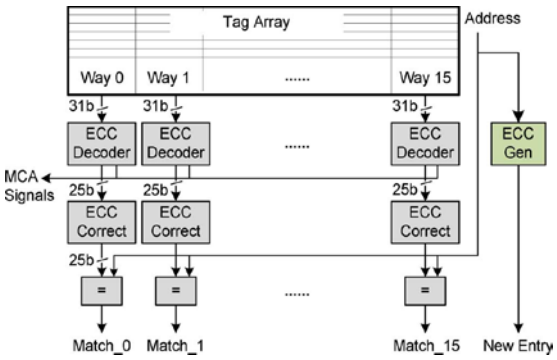

Fig. 1 Original data flow of a cache array lookup [2]

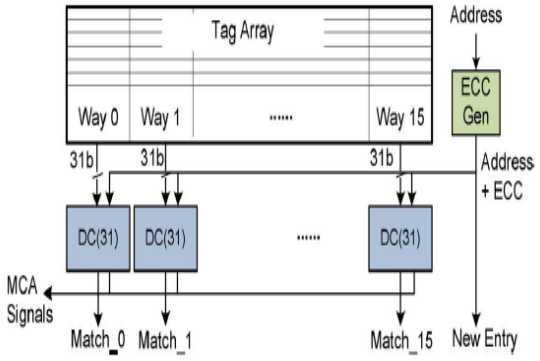

Fig. 2 New tag lookup circuit with the direct compare[2]

2.3 BWA BASED ENCODER DESIGN

In this design, the overall latency is reduced by performing the ending process to generate the parity bits from the incoming tag along with the tag comparison.

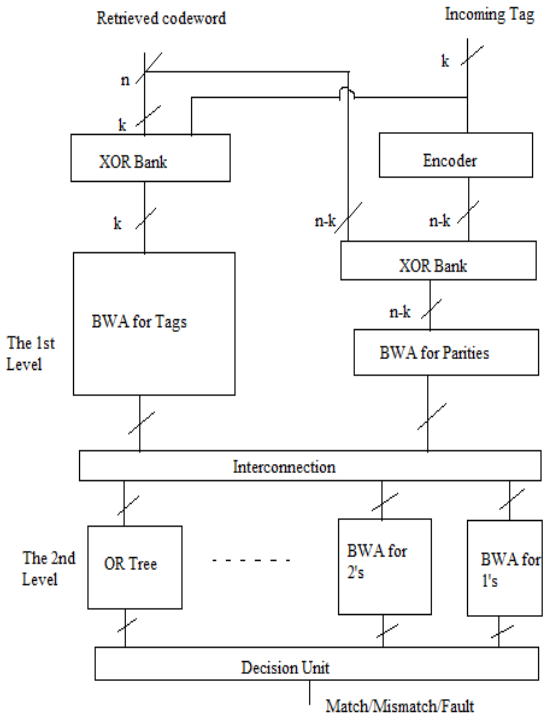

Fig. 3. BWA based architecture optimized for systematic codewords[1]

Fig. 3 shows the BWA based architecture optimized for systematic codewords which contains multiple butterfly-formed weight accumulators (BWAs) to improve the latency and complexity of the Hamming distance computation. For counting the number of ones among its input bits uses BWA and it includes multiple stages of HAs where each output bit of a HA is associated with a weight. In order to accumulate the carry bits and the sum bits of the upper stage separately the HAs in a stage are connected in a butterfly form. .

In fig. 3 produces a bitwise difference vector for either data bits or parity bits, and the following processing elements count the number of 1's in the vector, in each XOR stage. ie., the hamming distance. At the first level of each BWA generates an output from the XOR banks and several weight bits from the HA trees. Such outputs are fed into their associated processing elements at the second level in the inter connection. The subsequent OR-gate tree

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at the second level, is connected to the output of the OR gate tree and according to their weights the remaining weight bits are connected to the second level BWAs. The corresponding first and second level circuits are illustrated in fig . 4.

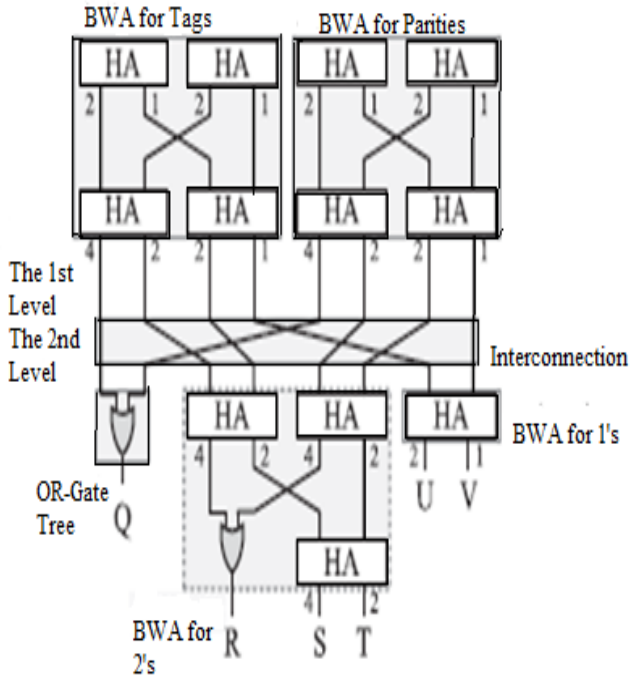

Fig. 4. First and second level circuits for a (8,4) code [1]

Table .1 :Truth table of the decision unit for a (8,4) code[1]

Q OR R OR S	*T*	*U*	*V*	*Decision*
0	*0*	*0*	*x*	*Match*
	0	*1*	*x*	*Fault*
	1	*0*	*0*	*Fault*
	1	*0*	*1*	*Mismatch*
	1	*1*	*x*	*Mismatch*
1	*x*	*x*	*x*	*Mismatch*

For the sake of simplicity, in fig.4 the Encoder and XOR banks are not drawn. The bits which have weight 4 are ORed. The extra bits which have weight 2 or 1 are connected to their corresponding BWAs. The decision unit finally determines if the incoming tag matches the retrieved codeword by taking the outputs of the preceding circuits. Thus, the decision unit is a combinational logic that takes the outputs of the preceding circuits as inputs and the functionality is specified by a truth table. For the (8,4) code the truth table for the decision unit is described in Table .1.

3. Proposed Design

Using modified half adder (HAM) and modified XOR gate (XORM).\ the BWA circuitary is replaced. XORM has 1 gate less than the conventional XOR gate of 5 gates (AND-OR-NOT implementation). HAM has 2 gates less than the conventional half adder. Thus, the area is reduced according to the number of number of gates reduces. The delay also reduced than conventional circuitry by using this XORM and HAM in BWA based encoder circuitry.

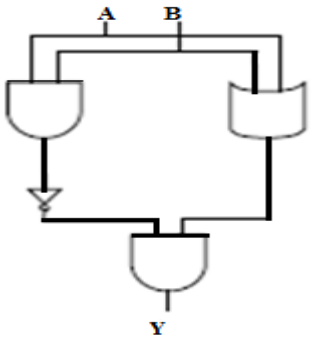

Fig 5. Modified XOR gate (XORM)

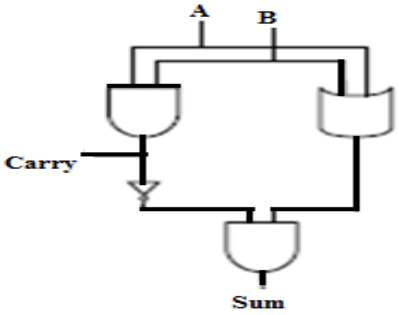

Fig 6. Modified half adder (HAM)

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4. Result

4.1 Simulation Result

Simulation was done in Xilinx 13.2.

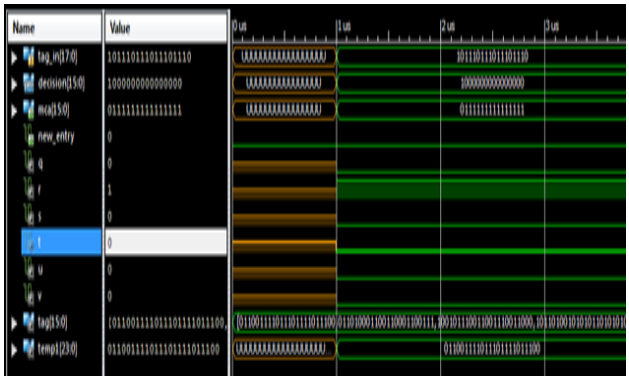

Fig. 7 Modified BWA based encoder circuitry for matching

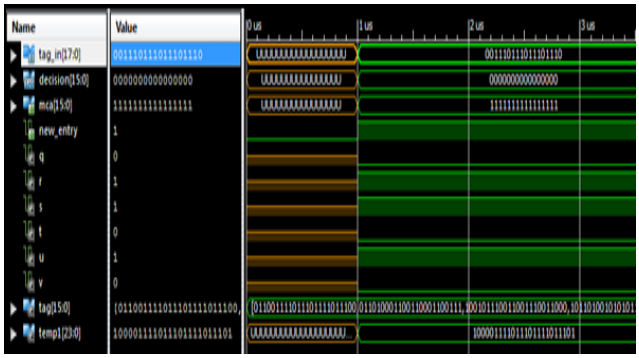

Fig. 8 Modified BWA based encoder circuitry for faulty input

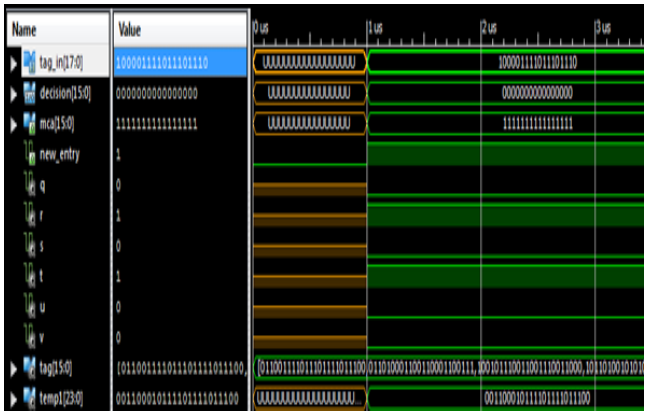

Fig. 9 Modified BWA based encoder circuitry for mismatching input

Table .2 Comparison table

	Area(A)	Delay(ns) (D)	Area-delay product(A*D)
Decoder circuitry	625	35.49	22181.25
SA base encoder circuitry	378	24.98	9442.44
BWA based encoder circuitry	313	23.36	7311.68
Modified BWA based encoder circuitry	249	20.86	5194.14

5. Conclusions

In this paper BWA circuitry replaced using modified half adder (HAM) and modified XOR gate (XORM) and it is simulated in xilinx 13.2. Simulation results shows that using this XORM and HAM in BWA based encoder circuitry, area and delay can be further reduced than conventional circuitry.

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Ms. Gopika Nath. G, received her B.Tech degree in applied electronics and instrumentation from Saint Gits College of Engineering, Kottayam, India, in 2013 and pursuing MTech in VLSI and Embedded system in Mangalam College of Engineering, Kottayam, India.

Ms. Hima Sara Jacob, Assistant professor at Mangalam College of Engin-eering,Kottayam,India.She completed her B-Tech in applied electronics and instrumentation from Saint Gits College of Engineering, Kottayam, India and received her M.Tech in VLSI and Embedded system from Saint Gits College of Engineering,Kottayam,India.

Reneesh.C.Zacharia received an Mtech degree in electronics and communication with specialization in VLSI design.He is currently working as an assistant professor at Mangalam College of Engineering Kerala,India