IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 12, December 2015.
www.ijiset.com
ISSN 2348 – 7968

The Ratio Growth In Profile Of Cobalt Silicide And Titanium Silicide And The Effect Of Them On Electrical Characterization For Nano Nmos Devices

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Abstract. This paper described on the growth process of the two silicide Sub-nanometer devices applied silicide growth on the top of polysilicon in order to produce better devices. In CMOS device gate, metal silicide is developed on-top of the polysilicon to produce a better ohmic contact compared to metal-polysilicon borders. Titanium silicide is formed by depositing PVD Ti on silicon substrates by annealing. Anneals were carried out in an N_2 ambient and resulted in at thin TiN layer on the silicide surface. To produce cobalt cilicide, a CVD cobalt layer was deposited on silicon at 450°C, after annealing it was found that no metal rich Co_2Si phase formed, at 800°C the high resistivity CoSi phase formed as the anneal temperature increased to 950°C, $CoSi_2$ formed. The high temperature required to form a silicide and the non existence of the Co_2Si phase are attributed to the oxide at the interface.. It is found that cobalt silicide grew faster and deeper to the silicon, thus saving a lot of time and cost. Further experiments also show that cobalt silicide has better electrical property such as sheet resistance, capacitance and electron mobility.

Keyword : Silicide, Titanium, nanometer, NMOS

INTRODUCTION

When Complimentary Metal-Oxide Semiconductor (CMOS) device scaling reached the submicron regime, a lot of complications surfaced. This is due to the non-linearity of the physicals and electrical characteristics of the materials in the device at such a small size. Approaching 65 nanometers, the electrical performance of silicon is at the extreme limit. At this region, the mentioned non-linearity gets complicated making it hard to set the fabrication recipe. One of the most important output parameters is the V_{TH} value. V_{TH} is one of the main parameters in determining whether the transistor works or not H.Elgomati et. al (2015). However, there is no single factor that can control the V_{TH} value when we scale down the device. Previous downscaling research conducted by Toshihiro Sugii et. al., (2003) showed multi-effects to the device performance such as short-channel-effect, Drain-induced Barrier Lowering (DIBL), punch through, and etc. These problems caused by many varying factors like gate oxide thickness, active area doping, halo implantation doping and many more. One of a main factor in getting a working transistor is to get a working gate. In CMOS, polysilicon gate is widely used. For sub-nanometer (less than 100nm) devices applied silicide growth on the top of polysilicon in order to produce better devices. A silicide is a compound that has silicon with more electropositive elements. Metal such as tungsten, titanium, cobalt, and nickel, is alloyed with the top layers of the polysilicon. This is to produce an ohmic contact between aluminum metal wire and polysilicon. This is very important to get the correct transistor characteristic. This paper discuss the comparison in growing titanium silicide and cobalt silicide, looking at two main area, the growth time, which translate to fabrication cost, and also the electrical characteristic of both, which translate to the device performance.

ISSN 2348 – 7968

SILICIDE TECHNOLOGY

Polysilicon is not an ideal conductor (approximately 1000 times more resistive than metals) compared to metal. The result is a reduction the signal propagation speed through the material. The resistivity can be lowered by increasing the level of doping, but even highly doped polysilicon is not as conductive as most metals. In order to improve conductivity further, sometimes a high temperature metal such as tungsten, titanium, cobalt, and more recently nickel, is alloyed with the top layers of the polysilicon. The resulting blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than polysilicon alone, because the silicide material is not near the channel. The process in which silicide is formed on both the gate electrode and the source and drain regions is sometimes called salicide, self-aligned silicide. The term salicide refers to a technology used in the microelectronics industry used to form electrical contacts between the semiconductor device and the supporting interconnect structure. The salicide process involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes. The term "salicide" is a compaction of the phrase self-aligned silicide. The description "self-aligned" suggests that the contact formation does not require lithographic patterning processes, as opposed to a non-aligned technology such as polycide. The term salicide is also used to refer to the metal silicide formed by the contact formation process, such as "titanium salicide", although this usage is inconsistent with accepted naming conventions in chemistry. The salicide process begins with deposition of a thin transition metal layer over fully formed and patterned semiconductor devices (e.g. transistors). The wafer is heated, allowing the transition metal to react with exposed silicon in the active regions of the semiconductor device (e.g., source, drain, gate) forming a low-resistance transition metal silicide. The transition metal does not react with the silicon oxide and or nitride insulators present on the wafer. Following the reaction, any remaining transition metal is removed by chemical etching, leaving silicide contacts in only the active regions of the device. A fully integrable manufacturing process may be more complex, involving additional anneals, surface treatments, or etch processes.

Figure below shows an example of salicide process flow

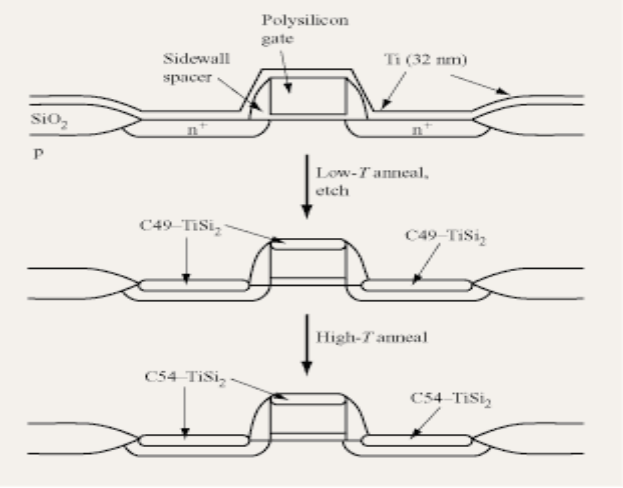

Figure 1 – Salicide Process Flow

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THE EXPERIMENT

Titanium silicide was the first material to be broadly used for logic applications. TiSi2 is typically formed with annealing titanium and silicon layer at 650C for 30s. To get a lower resistivity compound, the anneal process is being performed at 850C for 20s. As line widths and silicide thickness are reduced, it becomes increasing difficult produce a good structure due to the nature of big titanium atoms. This resulting in an imperfect electrical characteristic for the gate. Cobalt silicide was selected as the successor to $TiSi_2$ for its improved scaling to narrow line widths. However, in this paper, we just want to compare the growth rate and the resulting transconductance of the Cobalt silicide and Titanium silicide.

In this paper, a working 65nm NMOS transistor fabrication is used. In the salicide process step, cobalt and titanium are being alternate. The temperature is set at 1000C and the anneal time are varied to 18, 36 and 72 sec. Then we measure the thickness of silicides produced and also measure the transconductance of the polysilicon gate. That value would tell us the resistance in the silicide and as we know, we always want to get the smallest possible value. A graph is then plotted to see the relationship of varying anneal time to the resistance of the transistor polysilicon gate.

RESULT AND ANALYSIS

After fabricating the first transistor, which is using cobalt as silicide, with anneal time of 36 second, the resulting polysilicon gate is shown below

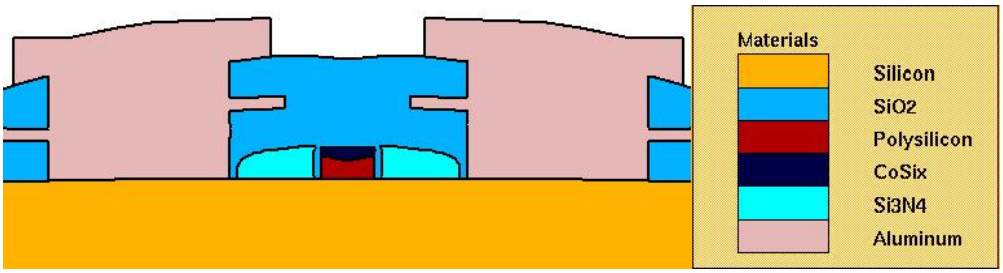

Figure 2 – Resulting Polysilicon Gate with Cobalt Silicide

As we can see, cobalt penetrates deep into the polysilicon, about 30%. This can be clearly seen in the zoom-in below

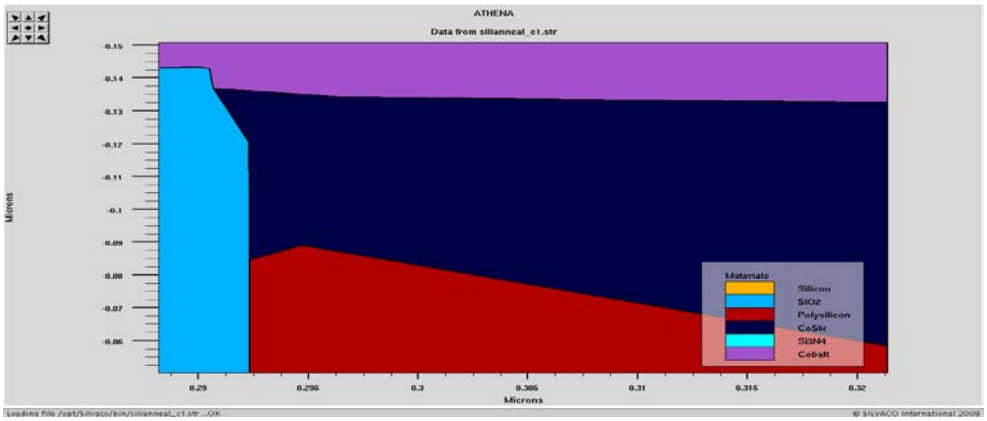

Figure 3 – Cobalt Silicide with 36 sec Annealing

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The depth of the silicide is about 0.0755 micron. The resulting resistance plot is

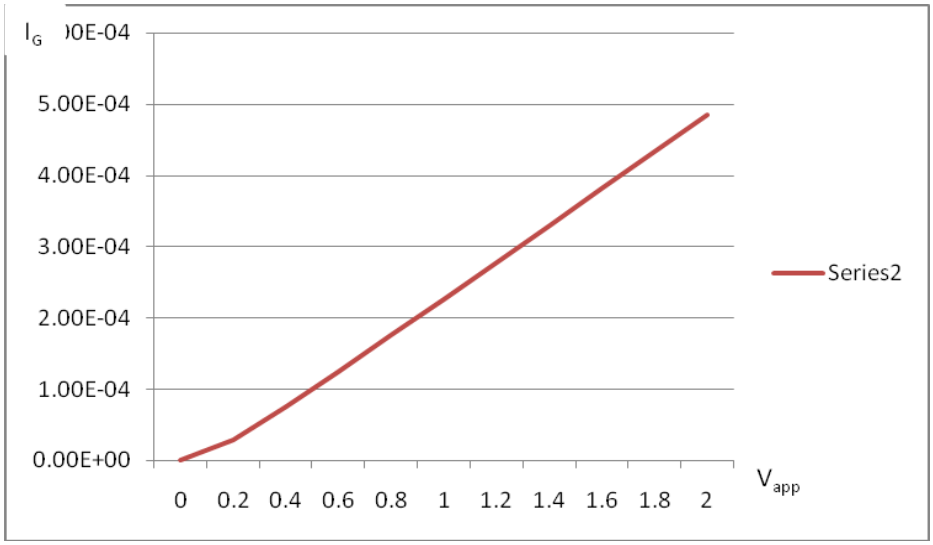

Figure 4 – Transconductance of the Set 1 Cobalt Silicide

From the graph, the transconductance value is 3993 mho with resistance at 0.000250 ohm. The value shows that the polysilicon gate acts almost like metal. For the nickel silicice transistor, the structure of gate with similar anneal time of 36 sec is

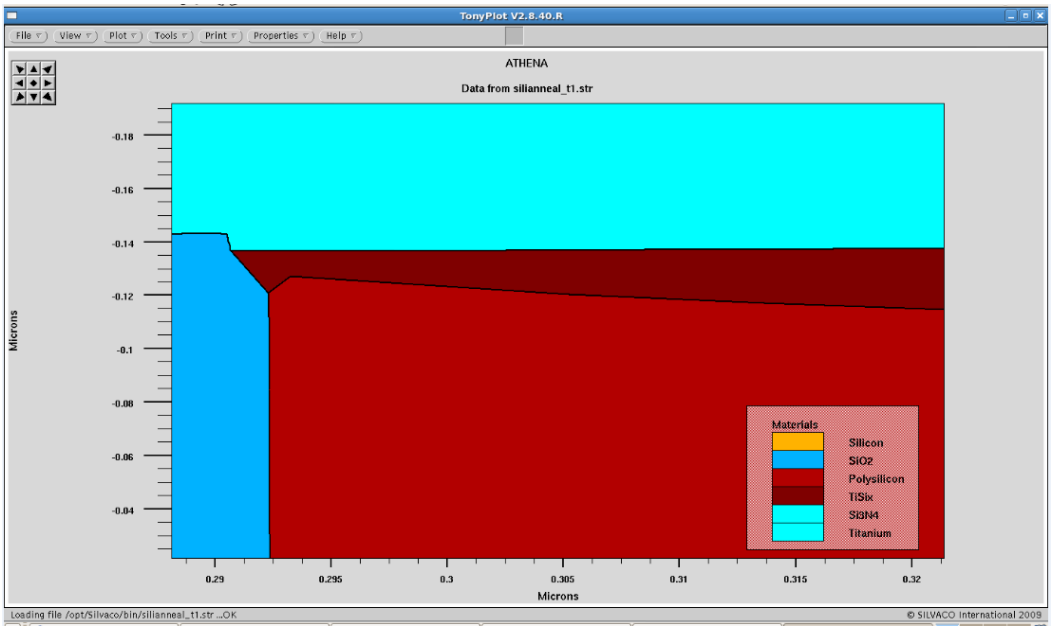

Figure 5 – Titanium Silicide with 36 sec Annealing

The depth of the silicide is about 0.0255 micron which is about a third of cobalt silicide thicness despite larger titanium atom. The resulting resistance e plot is

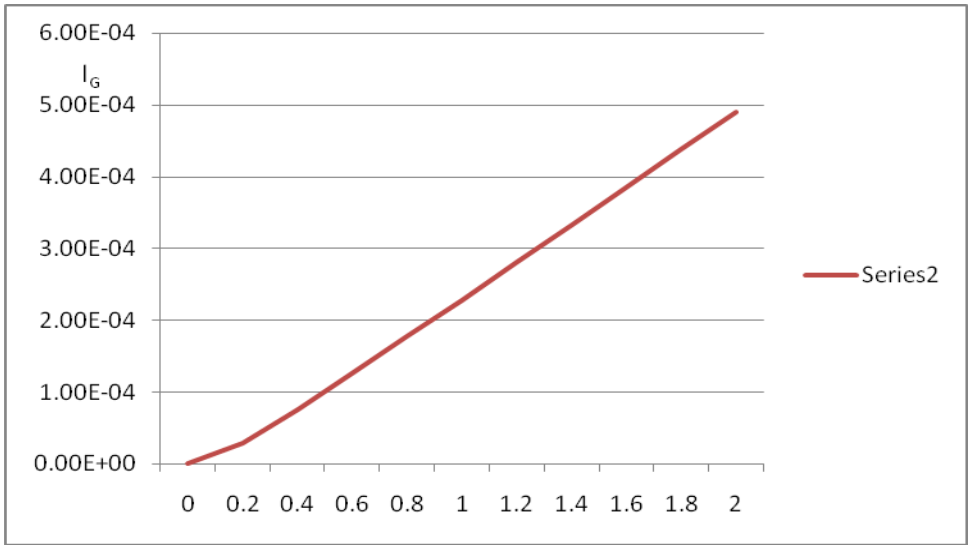

Figure 6 – Transconductance of the Set 1 Titanium Silicide

From the graph, the transconductance value is 3953 mho with resistance at 0.000253 ohm. This is slightly worse that cobalt silicide transconductance result.

As we run six set of fabrications, the resulting resistances can be seen as in table below and graph below

	Cobalt			Titanium		
Set	c5	c1	c2	t5	t1	t2
Anneal Time (s)	18	36	72	18	36	72
Resistance (ohm)	0.000252	0.00025	0.000247	0.000254	0.000253	0.000252
Transconductance (mho)	3961.824	3993.383	4046.838	3934.398	3953.593	3975.776

Table 1 – Experiment Results

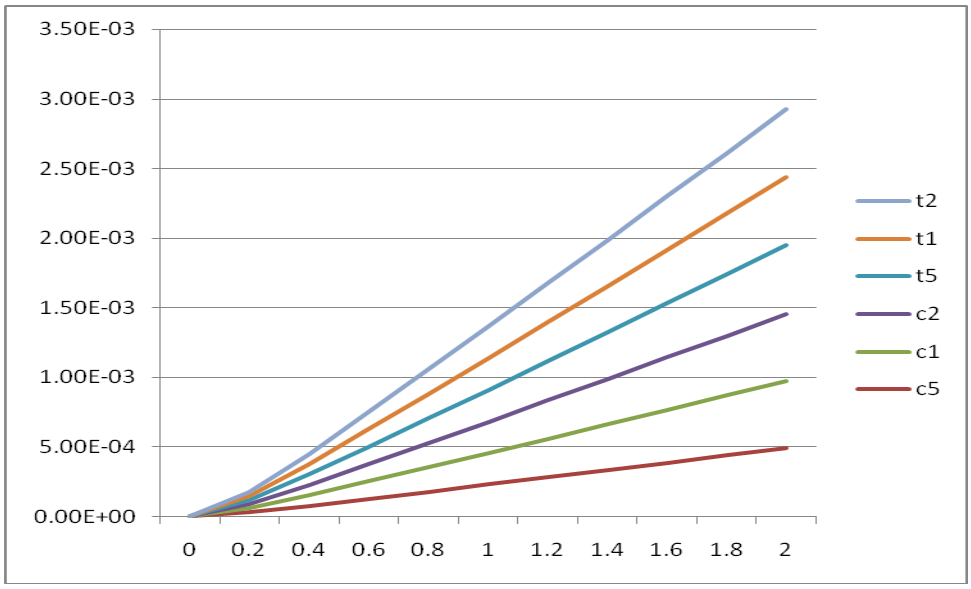

Figure7 – Transconductance of the Six Sets of Fabrication

The graph clearly shows that cobalt silicide has a better resistance compared to the titanium silicide. It also shows that, increasing annealing time in cobalt silicide will also result in bigger resistivity changes. As such, in a same process, cobalt silicide is clearly a more suitable silicide.

CONCLUSION

This project proves that cobalt silicide reacts more significantly to anneal temperature changes compared to titanium silicide. Cobalt penetrates much deeper to the polysilicon layer thus producing a thicker metal-like layer on the top of the gate. This in return, will produce a better ohmic contact for the gate thus making a better and faster transistor. However, there are many more consideration need to be made before selecting the right salicide process.

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