IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 12, December 2015.
www.ijiset.com
ISSN 2348 – 7968

Designing Of A New Low Voltage CMOS Schmitt Trigger Circuit And Its Applications on Reduce Power Dissipation

Milad Kaboli

Department of Electrical Engineering, Omidiyeh Branch, Islamic Azad University, Omidiyeh, Iran

ABSTRACT

The CMOS device is used to achieve better performance in terms of speed, power dissipation, size, reliability and hysteresis. Schmitt trigger minimized power consumption and improving compatibility with low voltage power supplies and analog component the most effective solution is to reduce the power consumption. The new proposed Schmitt trigger circuit is suitable for mixed-voltage input–output interfaces to receive input signals and reject input noise and also reduce fall time-rise time delay to decrease power dissipation. The proposed Schmitt trigger has been designed using 0.18 μm 1.2V CMOS technology and analyzed using PSPICE with BSIM3V3 device models.

Keywords: Schmitt trigger, hysteresis, aspect ratio, noise reduction, low power, power dissipation reduction.

1. INTRODUCTION

Digital circuit does not directly suitable for defining the digital signal, for some reasons it may have slow rise or fall time and may have the small noise sense by proceeding circuitry, so all of these critical conditions required a specified device that will “clean up” or maintain a signal the required device is known as the Schmitt trigger [1], output state depends on input state and changes only as input level crosses a preset threshold level. Schmitt trigger device is mostly used in analog and digital (0 or 1) circuit as wave shaping device to resolve the noise problem [2], This device is widely used to drive the load with fast switching low power loss and low power supply [3]. Schmitt trigger has been used irrelevant to improve on/off (0 or 1) control state [4], and reduce the sensitivity to noise, for example, sensor [3], pulse with modulation circuit [6].

2. DESIGN OF PROPOSED CMOS SCHMITT TRIGGER

Design of Schmitt trigger which covers transient as well as dc analysis will be discussed in this chapter [2]. Effect of W/L on hysteresis curve will also be discussed. The Schmitt circuit is a general inverter circuitry (double transistor inverter) with two extra transistors for providing the hysteresis. The double transistor inverter is used because the transistors (M2 and M5) have some higher threshold voltage than M1 and M4 due to body bias effect and due to which the output switches to high from low or low from high when after the ON condition of M2 or M4 respectively.

Now after addition of two more transistors M9 (M10) and M11 (M12) the circuit is capable to provide hysteresis [3]. When 0 input voltage is applied at the input, both M1 (M2) and M3 (M4) are in OFF condition while M5 (M6) and M7 (M8) are in ON condition and output is at high logic level. When the input reaches to threshold voltage of M1(M2) transistor then M1 (M2) will be on , while M3 (M4) remains OFF and at this time output will be high M9 (M10) will be on , so M1(M2) Try to pull down the

node between M1 and M3 while M9 (M10) try to pulls up this node to voltage VDD-VT , so transistor M3 (M4) stays the output to HIGH logic level , now when the input rises up to the threshold voltage of M3 (M4) then output switches to low logic level, so effectively our switching point shifted to higher voltage referred as VIH. Similar in case when input is falling from higher logic level then PMOS‘s comes into picture and switching point at output is shifted to some lower voltage referred as VIH. The difference between the VIH and VIL is referred as HYSTERISIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output , the output logic level‘s will remain same. Similar in case when input is falling from higher logic level then PMOS‘s comes into picture and switching point at output is shifted to some lower voltage referred as VIH. The difference between the VIH and VIL is referred as HYSTERISIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output , the output logic level‘s will remain same. If we examine the conditions from transistors (M1, M2, M3, M4, M9, M10). When output switches from high to low just before that: M23 (M4) in off condition. M1(M2) and M9 (M10) in saturation condition.

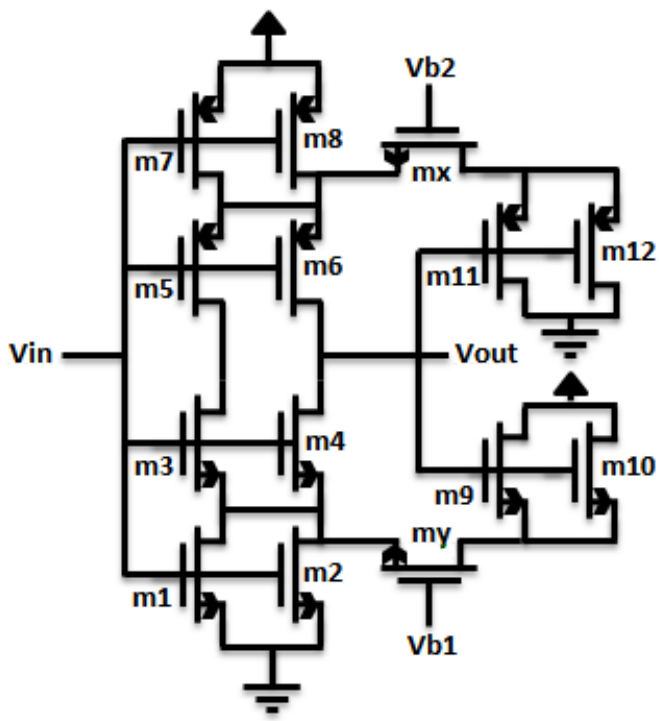

Fig. 1. Proposed Circuit to Improve fall time-rise time and Hysteresis Width

$$ID9 = K9/2\,(VGS - VTH9)^2$$

$$ID9 = K9/2\,(VDD - (Vin - VDSY - VTH3) - VTH9)^2$$

$$ID9 = K9/2\,(VDD - Vin + VDSY + VTH3 - VTH9)^2$$

$$VTH9 = VTH3$$

ISSN 2348 – 7968

$$ID9 = K9/2\,(VDD - Vin + VDSY)^2$$

$$ID1 = K1/2\,(VGS - VTH1)^2$$

$$ID1 = K1/2\,(Vin - VTH1)^2$$

$$ID1 = ID9$$

$$K1/2\,(Vin - VTH1)^2 = K9/2\,(VDD - Vin + VDSY)^2$$

$$VDD - Vin + VDSY = \sqrt{K1/K9}\;(Vin - VTH1)$$

$$Vin = \frac{\left[VDD + VDSY + \sqrt{\frac{K1}{K9}}\,VTH1\right]}{1 + \sqrt{\frac{K1}{K9}}}$$

This Vin is called VIH. Now Similarly for the VIL. Transistors M4 and M6, will be in saturation.

$$ID11 = K11/2\,(VSG - |VTH11|)^2$$

$$ID11 = K11/2\,(0 - (Vin - VDSX - VTH5) - |VTH11|)^2$$

$$VTH5 = VTH11$$

$$ID11 = K11/2\,(Vin - VDSX)^2$$

$$ID7 = K7/2\,(VSG - |VTH7|)^2$$

$$ID7 = K7/2\,(Vin - VDD - |VTH7|)^2$$

$$ID7 = ID11$$

$$K7/2\;(Vin - VDD - |VTH7|)^2 = K11/2\,(Vin - VDSX)^2$$

$$Vin = \frac{\left[VDD + |VTH7| - \sqrt{\frac{K11}{K7}}\,VDSX\right]}{1 + \sqrt{\frac{K11}{K7}}}$$

The circuit designed for = 2V and =3 is shown in Fig. 1. Results are shown in Fig. 2 and Fig.3.

In proposed circuir with change VB1 and VB2, Hysteresis Width can be tuned. Voltage of VB1and VB2 are about vcc.

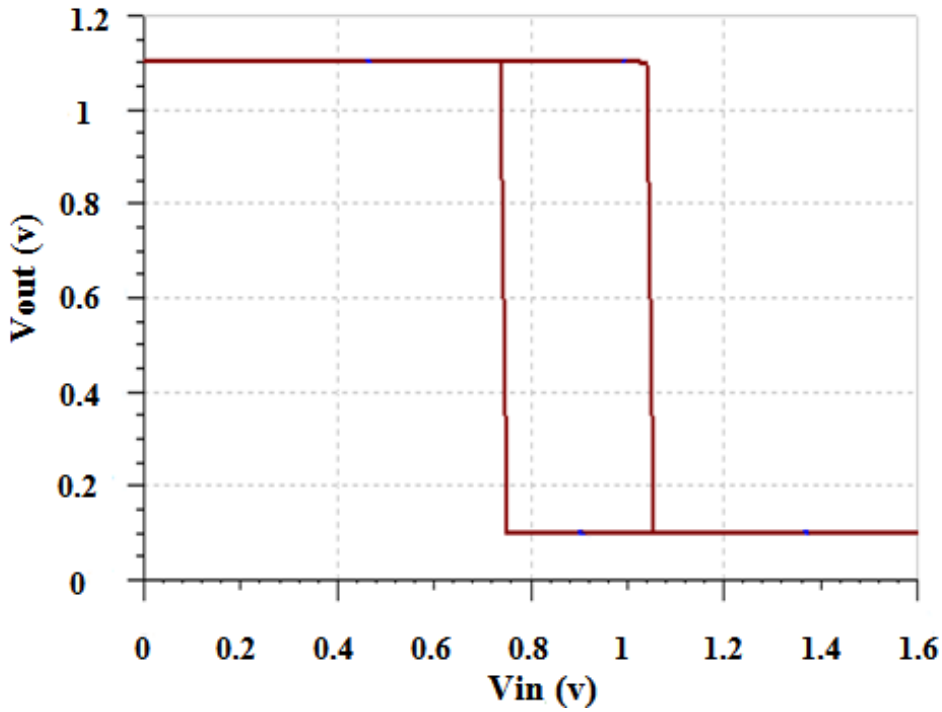

Fig. 2. Voltage Transfer Charachterisric (VTC)

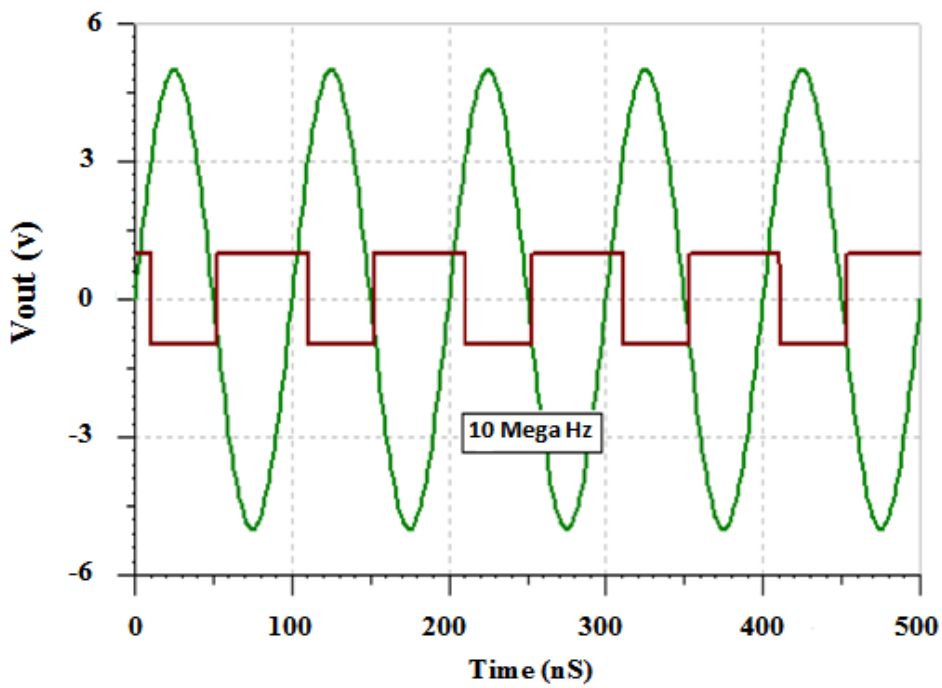

Fig. 3. Time Domain Analysis

3. EFFECT OF VARIATION OF W/L RATIO OF TRANSISTORS ON HYSTERESIS CURVE

On increasing the W/L of transistor M1(M2) the curve will shift towards the LEFT side, because in this case our NMOS will strong and pulls the output sharply to low logic level. Second case when M7(M8) will strong then it will maintain the output to logic level high for greater duration so the curve will shift to RIGHT side. There will no effect on the hysteresis curve on changing the sizes of transistors M3(M4) and M5(M6). This can be also verified from the equations derived for VIH and VIL in previous section.

If the size of transistor M9(M10) is increased then it will affect only on VIH level, because when we increase from low to high then lower portion of SCHMITT comes into picture to control the VIH level, hence by increasing the size the VIH will increase while in same way transistor M11(M12) affect only on VIL level. When size of M11(M12) is increased then VIL will be reduced. We can also conclude that the aspect ratio of M7(M8) and M7(M8) transistors affect the VIL level while the aspect ratio of M1(M2) and M9(M10) affect the VIH level. The area of hysteresis curve determines the amount of noise immunity provided be the circuit. Greater the difference between the VIH and VIL level means more immunity.

4. SIMULATION RESULTS:

For the simulation of proposed circuit BSIMV3 Ver 3.1 models of TSMC 0.18µm CMOS process were used. Simulations results are reported in Table 1. These results show that fall time-rise time is achieved with modified Schmitt Trigger.

Table 1. Comparison between Power Dissipation OF Conventional CMOS

Tr & Tf (nS)	Power Dissipation OF Conventional CMOS inverter Without Schmitt Trigger (µW)	Power Dissipation OF Conventional CMOS inverter With Schmitt Trigger (µW)
10	1.43	1.56
12	1.87	1.98
14	1.93	2.02
16	2.13	2.20
18	2.29	2.32
20	2.40	2.40
40	3.14	3.02
60	5.21	4.89
80	6.56	5.89
100	8.78	6.35

REFERENCES

1. H.Morimura, T. Shimannura, K. Fujii, S. Shigematsu, Y. Okazaki and M. Katsuyuki, "A zero sink current schmitt trigger and windows flexible counting circuit for fingerprint sensor/identifier" IEEE International Solid State Circuit Conference (ISSCC), Vol. 1, pp.122-517,2004.
2. S.L, Chen and K.Ming-Dou, " A new Schmitt trigger circuit in a 0.13µ 1/2.5v CMOS processes to receive 3.3 v input signals," IEEE Transaction on circuits and System 2; Express Briefs, Vol.52, issue 7.pp.361-365,2005.
3. Pedroni, "LOW-Voltage high speed Schmitt trigger and compact windows comparator," IEEE Electronics Letter, Vol.41, no.22, 1213-1214, 2005.
4. H. Mangalam and K. Gunavathi, " Gate and subthreshold leakage reduction SRAM cells", DSP Journal 6, Issue 1, September, 2006.
5. H. Kim, H.J.Kim and W.S.Chung, "Pulsewidth modulator circuit using cmos Oats," IEEE Transactions on Circuit and System 1; Regular papers, Vol.54, pp.1869- 1878, sept. 2007.
6. C. Kho Pham "Cmos Schmitt Trigger Circuit with controllable hysteresis using logical threshold voltage control circuit" IEEE Vol.36, No.1821-1824, 2007.
7. CMOS: circuit design, layout, and simulation, Volume 1 by R. Jacob Baker.
8. [3] J. P. Uyemura, Circuit Design for CMOS VLSI.