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Literature Survey On RFU for flexibility

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Abstract

Reconfigurable instruction set processor refers to the architectures which consisting of both microprocessor as well as reconfigurable logic. Both the software flexibility and hardware efficiency is combined in RISPs.

This paper tells us about different application specific instruction set processor platforms which are compared according to their speed, compilation time, performance and energy to prove that reconfigurable instruction set processor has enough flexibility and efficiency.

Keywords-*reconfigurable instruction set processor, reconfigurable logic, and compilation time*

1. INTRODUCTION

General purpose processors can be utilized easily in embedded systems since general purpose processors are flexible, their design cost is low, tools availability and their programmability. For the case of high performance computation GPPs are not efficient. So to enhance performance and to improve energy efficiency ASICs(Application specific integrated circuits) came into picture. But the design cost of ASICs as well as turnaround time[1] is high so ASIP(Application specific integrated processor) are proposed. In case of ASIPs the critical portion of any application are accelerated by using the custom functional units. But compared to ASICs ASIPs are not that effective. Programmability and flexibility is maintained compared to ASIPs but ASIPs has two problems they are increasing algorithm complexity as well as design cost.

So to overcome the problems which are seen in ASIPs ,RISP came into picture. RISPs are similar to ASOPs here the most repetitive as well as time consuming parts of an application are run on the dynamic, adaptive functional unit called as RFU(reconfigurable functional unit)[2].

During runtime, expansion of instruction set architecture is possible with the usage of RISP. According to the market shifts and evolving standards in the market RISP can be designed.

This paper surveys about different application specific processors which are coupled with reconfigurable functional unit. How RFU can improve performance, speed , energy and compilation time in these processors are observed.

2. LITERATURE SURVEY

2.1) Low power coarse grained reconfigurable instruction set processor

Mainly how power is saved using coarse-grained reconfigurable processor is presented in this paper[3].

Here to decrease power consumption, division of reconfigurable logic is done into slices such that they can be activated separately. This reconfigurable processor is designed in such a way that compared to RISC processor the performance and energy of this processor is greater than 2.5 times and 18% respectively.

2.2) A VLIW processor with reconfigurable instruction set for embedded applications

This paper[4] presents one of the application specific processor which is tightly coupled with reconfigurable unit. Specific architecture model is described in this paper[4], which is XiRISC(extended Instruction set RISC), It has VLIW processor coupled with instruction level parallelism. It is flexible in such a way that it can support wide range of applications. It supports for executing DSP functions, telecommunication, elaboration in multimedia etc…

Compared to low power embedded processor it can reduce energy consumption so that power is saved compared to earlier cases. Up to 92% energy consumption can be reduced and even 4.3x to 13.5x speed ups can be increased with the use of this processor.

2.3) Chimera: A high performance architecture

This paper[5] presents one more application specific processor which is tightly coupled with reconfigurable

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functional unit. But here RFU unit is small and fast. The processor used here is super scalar processor.

This paper[5] deals with the study of performance of chimera. Under both optimistic and pessimistic assumptions the parameters such as timing, speedups and performance are studied. The presented micro architecture is capable of mapping a set of instruction sequence to RFU. For a single RFU operation 9 registers for input and 1 register for output is needed. After modelling it is observed that speedups is in between 31% for optimistic and 21% for pessimistic respectively.

Using automatic compilation of Chimera improvement in the performance can be observed.

2.4) Multi reconfigurable instruction set processor system on chip

To increase the performance new processor was designed reconfigurable functional unit. Since RFU is flexible and efficient, this paper presents details of MRPSOC. In this platform[2] applications can be run parallel, the performance can be enhanced due to reconfigurable functional unit present in it.

In order to improve the performance both methods of RISP and MPSOC is considered. By using these methods in common platform at the two levels competition time can be reduced. Programs are executed simultaneously on the parallel processing units at the first level. Execution time is reduced by running the complex section of task on the RFU at the second level.

The RFU which is proposed in this paper has multiple functional unit which are organized as matrix. All types of MIPS instructions are supported by these functional units except multiplication, division, store and load.

The cost of IC can be reduced; the proposed RFU is flexible and efficient. About 40.90% completion time can be improved compared to the homogeneous MPSOCs.

3. CONCLUTION

In this paper, different types of application specific processor which are coupled with RISPs can be seen [2],[3],[4],[5]. The speed performance, flexibility of all the processor are compared. Since MRPSOC is combination of MPSOC and RISC. In MPRSOC application can be run in parallel in processor and complex portions of the code can be executed in RFU the flexibility and efficiency is better.

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REFERENCES

[1] K. Keutzer, A. R. Newton, J. M. Rabaey, and A. SangiovanniVincentelli, "System-level design: Orthogonalization of concerns and platform-based design," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 19, no. 12, pp. 1523-1543, 2000.

[2] R.Soleymanpour, Siamak Mohammadi, “A Platform for Multi Reconfigurable Instruction Set Processor System on Chip”, in CSI International Symposium, 2013, pp.99-104

[3] F. Barat, M. Jayapala, P. O. de Beeck, and G. Deconinck, “Software pipelining for coarse-grained reconfigurable instruction set processors,” in *Proc. ASP-DAC*, pp. 338–344, Jan. 2002.

[4] A. Lodi, M. Toma, F. Campi, A. Cappelli, R. Canegallo, and R. Guerrieri, "A VLIW processor with reconfigurable instruction set for embedded applications," *Solid-State Circuits, IEEE Journal of,* vol. 38, no. 11,pp. 1876-1886,2003.

[5]”CHIMAERA: A High−Performance Architecture with a Tightly−Coupled Reconfigurable Functional Unit”, Zhi Alex Ye, Andreas Moshovos, Scott Hauck*, and Prithviraj Banerjee