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# FPGA-Based Intelligent Traffic Light Controller System Design

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***Abstract*** **— Growing numbers of road users and the limited resources provided by current infrastructures lead to ever increasing travelling times mainly because of use of traditional traffic light controllers. The Intelligent Traffic Light Control system proposed in this paper aims at reducing waiting times of the vehicles at traffic signals. Present Traffic Light Controllers (TLC) are based on microcontroller and microprocessor. The limitation with the existing TLC is that it uses fixed time slots, which is functioning according to the program that does not have the flexibility of modification on real time basis. This proposed system makes use of FPGA technology along with traffic sensors to control traffic according to the traffic requirement and thus reduces the waiting time, at an intersection of two roads. The time intervals of the green, yellow and red states are based on real time traffic density, which optimizes traffic light timing and avoids traffic congestion, and it is an improvement upon the efficiency of the current Traffic Light Controllers. The system has been successfully tested and implemented in hardware using ALTERA Cyclone II- FPGA. The system has many advantages over the exciting TLC.**

***Index Terms*****--- ALTERA, Cyclone II- FPGA, Sensors, Traffic Light Controllers.**

## I. INTRODUCTION

Traffic congestion problem of roads especially in the urban cities is becoming worse as number of vehicles on the road is increasing day by day. The limited resources provided by current infrastructures are leading to ever increasing travelling times, making the safety and waiting time of road users a matter of grave concern.

The Intelligent Traffic Light System implemented in this project aims at minimizing the waiting times of vehicles at the traffic signals in a city.

Field programmable gate arrays (FPGAs) are extensively used in electronic systems, for rapid prototyping and verification of a conceptual design, especially when the mass-production of a conventional IC becomes prohibitively expensive due to the small quantity. Many electronic system designs that used to be built in conventional silicon VLSI are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mass production unit of a conventional VLSI especially for small quantity. Main objective of this paper is to design a real time 24-hour traffic light controller to manage the traffic movement of four roads at the same time, and achieve minimum waiting times for the road users. Our design senses the traffic with the help of sensors embedded on the roads and accordingly green light timings are changed to reduce the waiting times of the vehicles. In the rush hours, when people going to work or coming back to home the traffic lights of all roads are given more time to clear the heavy traffic. However, in slag period when traffic is not heavy the less time is given to clear the traffic. [1]

## II. STRUCTURE OF THE FOUR ROADS TO BE CONTROLLED

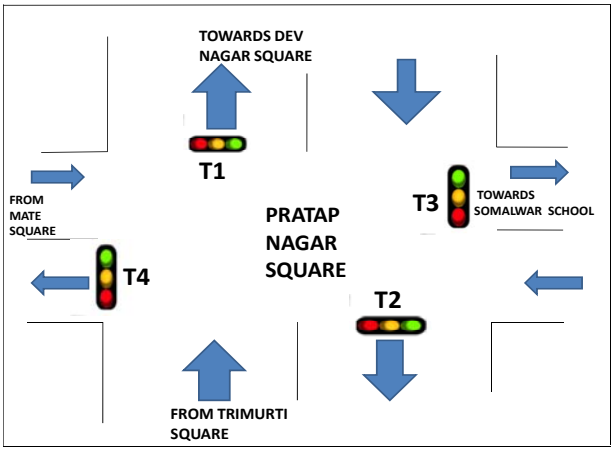


**Fig.1. The structure of the Square to be controlled.**

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**Fig**. 1 shows the structure of the four roads (square) that has been used as a practical example to design our controller which is located in **Nagpur city**, ***Maharashtra State, India***. In this structure we have four traffics, T1, T2, T3, and T4. The main roads are T1 and T3. The timing for the traffic's is working as follows:

- for dense traffic: T1 and T3 are green for 40 seconds & T2 and T4 are green for 20 seconds and green to yellow sign has 5 seconds delay.
– T1 will stay green for 40 seconds then it will turn to yellow for 5 seconds, then
–T2 will turn to green and remains green for 40 seconds, then it will turn to yellow for 5 seconds, then
–T3 will turn to green and remains green for 40 seconds then it will turn to yellow for 5 seconds then
–T4 will turns to green for 40 seconds and after that it will turn to yellow for 5 seconds,
--then the cycle repeats if the sensors output is still in logic '1' state.

Table I show timing states for the four traffic lights when the traffic is heavy and sensors output = '1'.

TABLE I. TIMING STATES OF TRAFFIC SYSTEM (PEAK HOURS)

| Time in Sec | T1 | T2 | T3 | T4 |
|---|---|---|---|---|
| 0 to 40 | Green | Red | Red | Red |
| 40 to 45 | Yellow | Red | Red | Red |
| 45 to 65 | Red | Green | Red | Red |
| 65 to 70 | Red | Yellow | Red | Red |
| 70 to 110 | Red | Red | Green | Red |
| 110 to 115 | Red | Red | Yellow | Red |
| 115 to 135 | Red | Red | Red | Green |
| 135 to 140 | Red | Red | Red | Yellow |

*Traffic control when roads are not crowed:*

When the roads are not crowded (output of all sensors is equal to logic '0'); the scenario of the traffic is as follows: (assuming that output of sensors have turned to logic '0' at the end of yellow period of T4 traffic).The system restarts with T1 having the green sign.
– T1 will stay green for 20 seconds then it will turn to yellow for 5 seconds, then

- for thin traffic: T1 and T3 are green for 20 seconds & T2 and T4 are green for 10 seconds and green to yellow sign has 5 seconds delay.

*Traffic control when roads are crowed*:

Assuming that the roads are crowded (output of all sensors is equal to logic '1'); the normal scenario of the traffic is as follows:–
The system starts with T1 having the green sign.
–T2 will turn to green and remains green for 20 seconds, then it will turn to yellow for 5 seconds, then
–T3 will turn to green and remains green for 20 seconds then it will turn to yellow for 5 seconds then
–T4 will turns to green for 20 second and after that it will turn to yellow for 5 seconds, then
–T1 will turn to green and cycle will repeat until the traffic reduces and sensors' output turn to 'one'.

Table II show timing states for the four traffic lights when the traffic is not crowded and sensors output is = '0'.

TABLE II. TIMING STATES OF TRAFFIC SYSTEM (SLAG HOURS)

| Time in Sec | T1 | T2 | T3 | T4 |
|---|---|---|---|---|
| 0 to 20 | Green | Red | Red | Red |
| 20 to 25 | Yellow | Red | Red | Red |
| 25 to 45 | Red | Green | Red | Red |
| 45 to 50 | Red | Yellow | Red | Red |
| 50 to 70 | Red | Red | Green | Red |
| 70 to 75 | Red | Red | Yellow | Red |
| 75 to 95 | Red | Red | Red | Green |
| 95 to 100 | Red | Red | Red | Yellow |

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## III. SIMULATION

Fig.2 Shows the simulation results for the controller with sensors output = logic '1', i.e. when traffic is crowded, the transition time will be more.

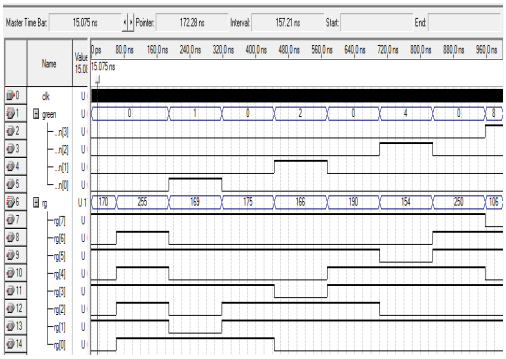

Fig.2. Simulation Results for the Controller when S ='1'

Fig. 3.Shows the simulation results for the controller with sensors output = logic '0', i.e. when traffic is slag, and the transi

tion time will be less.

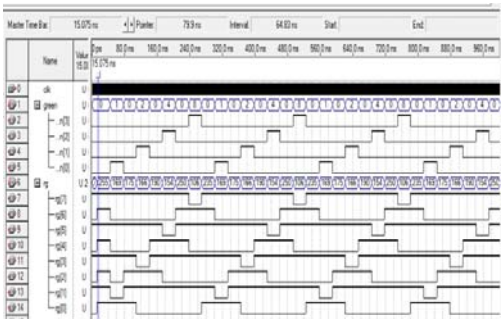

Fig.3. Simulation Results for the Controller when S ='0'

## IV. FPGA IMPLEMENTATION AND HARDWEAR MODEL

The wire loop embedded in the road can sense and respond to traffic on the road. Electric current, running through the loop, creates a magnetic field. When a car bumper interferes with this field, a signal is sent to a roadside traffic light controller and the timing of the traffic lights can be changed accordingly to minimize the waiting times of the cars.
The design of our traffic light system went through different stages. The first stage was the implementation of the state diagram. The second stage was writing the HHDL code. The third stage was simulating the VHDL code. The fourth stage was programming the FPGA and the last stage was the development of the interface circuit. The design has been tested on ALTERA Cyclone II- FPGA.
The system has been successfully implemented, tested and compared to the existing traffic lights at Pratap Nagar Square, Nagpur city, Maharashtra State, India Fig. 3. Shows the VHDL model of the controller,

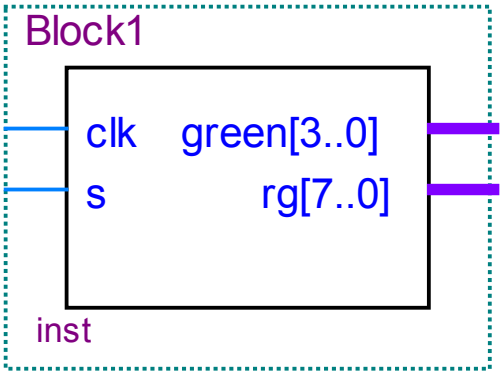


Fig. 3. VHDL Model of the Controller.

Where:
- **Clk:** Is the system clock.
- **S:** are Sensors used to sense the traffic.
- **green[3:0] :** represents the four green traffic lights that the system is going to control.
- **rg[7:0] :** represents the total seven traffic lights (four red & four yellow) that the system is going to control.

For example **T1 <2:0>** represents the (red, yellow and green) sign, where each color represents one bit (**T1 <2>** □ Green, **T1 <1>** □ Yellow and **T1 <0>** □ Red).

## V. CONCLUSION

An intelligent traffic light controller system using FPGA design for a four roads structure with four traffic lights, as shown in fig.1, has been simulated, implemented and tested. The system has been designed using VHDL, and implemented on hardware using Altera Cyclone II FPGA. The system is compared with the existing traffic lights systems and it is found that it reduces maximum up to 70 to 80 seconds waiting time of the vehicles at the square in slag hours of traffic. Our design reaches the maximum utilization of the traffic either during rush hours or slag time. More functions could be added to the design. Some of these functions are to control more than four traffic lights. Also, to allow the user to assign the time for each traffic light, adding more sensors on each road to count the number of vehicles in each road and check for the longer queue to increase the time for that road, another function is to link the traffic light with the other traffic lights along the streets to increase the flow of traffic by reducing overall waiting time.

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