IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 4, April 2015.
www.ijiset.com
ISSN 2348 – 7968

# A Review: High Speed Low Power Flash ADC

**Rahul D. Marotkar[1], Dr. Manoj S. Nagmode[2]**

[1]Department of Electronics & Telecommunication, MIT College of Engineering, Pune (MH), India

[2] Professor, Department of Electronics & Telecommunication, MIT College of Engineering, Pune (MH), India

**Abstract**

In computerized world, The Speed, area and power are critical variables for high velocity aplplications.ADC is a mixed signal system that changes over the analog signals to the digital signals for transforming the data. In present day CMOS innovation the flash ADC is composed by utilizing the dynamic method, it fundamentally diminishes the power, voltage and delay. A flash ADC is extremely valuable for fastest speed when it is contrasted with the other ADC architectures.ADC is attempting to contrast the simple information with an arrangement of levels. In digital signal processors it is persistently challenge analog designer to enhance and grow new ADC architectures.

***Keywords***: *ADC, Flash ADC, CMOS, Comparator, Encoder.*

## 1. Introduction

A survey of the field of flow A/D exploration uncovers that a dominant part of exertion has been coordinated to diverse sorts of architectures, having interesting attributes and distinctive limitations[2].The general piece outline of ADC is demonstrated in fig.1. It has continuous, infinite valued signal as its input. Out of those distinctive sorts of architectures, one of the speediest converter that is Flash ADC is likewise called as parallel ADC or direct change ADC to change over a simple to computerized sign [5-9]. That uses a straight voltage scale (set of stages) with a comparator at every level (Horizontal) of the scale to contrast the data voltage with the progressive reference voltage. It is exceptionally valuable to fast and huge transmission capacity applications like radar handling, advanced oscilloscope, audio, video and remote interchanges [15].

Paper association is as take after: In Section 2, we will examine the construction modeling of Flash ADC. In section 3, we review contrast goal of Flash ADC. At long last, in Section 4, we finish up the paper.

## 2. Architecture

The typical flash ADC block diagram is shown in fig.2. The flash ADC has been isolated into three noteworthy squares, resistor step, comparator and encoder. By and large for N-bit flash need to $2^N$-1 limits which are proportional to such a variety of comparators and $2^N$ resistors (a resistor string), the reference voltage (Vref) is partitioned into $2^N$ qualities and every value is nourished to the comparator [6-8]. The data voltage Vin is contrasted and every reference value and at the yield of the comparators. A thermometer code is produced. Contingent upon the level of info, no. of 0's and 1's keeps fluctuate much the same as mercury in thermometer and that is the reason this code is called as thermometer code.

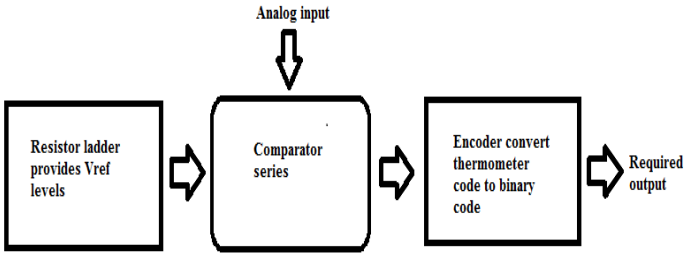


*Fig. 1:* Block Diagram of Flash ADC

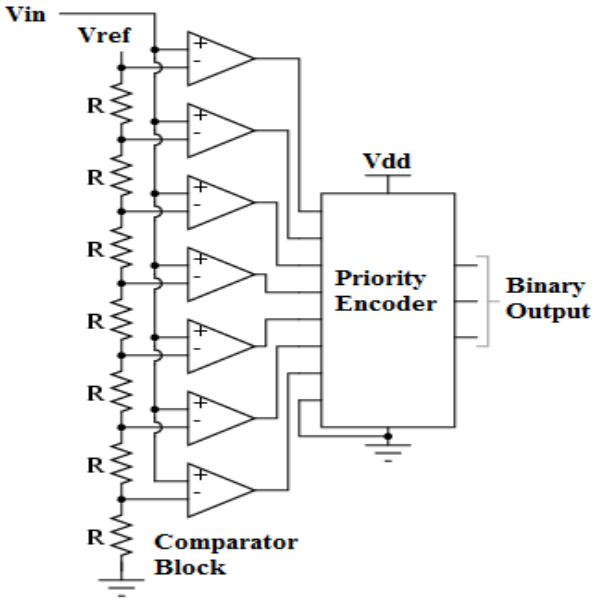


*Fig.2:* Flash ADC

ISSN 2348 – 7968

The thermometer code is an uncommon code despite the fact that we have $2^N$-1 bits, all conceivable bits successions are not permitted just those arrangements are permitted which are all 1's trailed by all 0's are permitted.[6] A basic $2^N$-1:N computerized thermometer decoder circuit changes over the looked at information into a N-bit advanced word. The primary point of interest of this converter is the rate with which one transformation can happen. Each clock pulse generates an output digital word. That is focal point of having high speed. Flash ADC converters have customarily been restricted to 8 bit determination having transformation rates of 10-90 Ms/s utilizing CMOS technology [2-3]. The bottlenecks of the flash ADC is to change over thermometer code to gray code(for a low power flash ADC)and convert the thermometer code to gray code(for reduce the effect of bubble errors). Quick input signals, small timing contrasts in the middle of clock and signal can result in bubbles in output code. If the determination builds the flash ADC obliges an expansive number of comparators therefore, number of comparator expands, the die size also increases and results a large amount of power dissipation [1].

## 3. Literature Survey

In this section, we survey on different methods and applications of high speed low power flash ADC.

George Tom Varghese and K.K. Mahapatra et al. [6] was proposed 5 bit streak ADC which is extremely effective low power encoder strategy for a gigahertz every example. In this paper, the encoder was composed in 90nm innovation with 1.2V force supply utilizing pseudo NMOS logic style to enhance the speed and reduce the power consumption furthermore decrease the bubble error which is produced because of test and hold circuit and sign delay. The normal power consumption was 0.3149mW.

Pradeep Kumar and Amit Kolhe et al. [10] introduced the outline of low power 3 bit flash ADC using 0.18 um technology with 1.3V force supply. This paper was proposed and clarified how the flash ADC is quick contrasted with other ADC structural planning furthermore clarified how it is inside codes extremely inefficient to hardware. So it is commonly just utilized as a part of uses where the latency is paramount and the hardware multifaceted nature is unassuming. The one restriction of the ADC converter is the exactness on account of simplicity of the circuits. For high resolutions the flash ADCs are very costly as a result of complexity is exponentially increments with the quantity of bits increments. The normal power consumption was 36.273 mW.

Mamta Gurjar and Shyam Akashe et al. [3] proposed the flash ADC converter for threshold inverter quantization with low power encoder. In this paper, proposed the fast ADC converter using fat tree encoder which is exceptionally suitable and precise. The comparator was outlined using TIQ technology. The TIQ technology gives high conversion speed and makes ADC faster.

K.Lokesh Krishna and T. Ramashri et al.[2] executed the Novel hybrid analog to digital converter which contains two stage quantizer has a flash ADC and SAR ADC with resistor ladder. Actually for rapid operation, flash ADC is utilized and for low power and high resolution, SAR ADC is utilized. By utilizing the flash ADC, we can enhances the speed and by using the SAR ADC we can accomplished the power decrease and resolution. To defeat the drawbacks, for example, low speed, hybrid ADC has been implemented. In this paper, the designed converter achieved great performance and it is suitable for high speed or high frequency applications.

P. Rajeswari, Dr.A.R.Aswatha and Dr.R.Ramesh et al. [4] proposed the low power design system for flash ADC. With the assistance of this technique we can reduced the power utilization of flash analog to digital converters when reduced the quantity of comparators by half. This paper was proposed the precision of the flash ADC by using the T/H circuit. Their proposed technique spared 35% of power consumption when contrasted and the conventional one.

Parthasarthy K.P. and, Dr. K.C.Narasimhamurthy et al. [1] proposed the usage of the low power consumption flash ADC for very high end receivers. The demanding issue in this paper was to design a low power latched comparator using 90nm technology with 0.8V DC supply. This technique consumes low power of 7.67mW, which consumes a low power of around half for a sampling frequency upto 1.2GHz. This configuration can be extended to high speed applications because comparator utilized as a part of this plan can work upto 5GS/s.

Kirankumar Lad and M.S.Bhat et al. [5] planned the flash ADC which accomplishes 5.76 ENOB at nyquist input frequency without adjustment. The INL and DNL are 0.08LSB and 0.1LSB individually. This technique consumes low power of 15.75mW with 1V supply and an energy efficiency is 0.29pJ/conv working at 1GS/s.

R Komar et al. [7] proposed a 0.5 V, 50 MS/s, 6 bit Flash ADC with 180 nm CMOS technology. In this design an inverter based comparator is used to reduce the silicon area and power necessity for a high low voltage operation low limit MOSFETs are used. For expanding the power effectiveness and speed of operation, a basic clock deferring technique and consecutive inverters in the comparators have been used. For digitizing comparator yields, A fat tree encoder design is used. The SNDR is

ISSN 2348 – 7968

31dB for the input frequency of 5.1MHz.The INL and DNL are 0.375LSB and 0.025LSB separately and power consumption is 0.3mW.

Timmy Sundstrom and Atila Alvandpour et al. [12] proposed a 2.5GS/s flash ADC planned in 90nm CMOS technology. Evades conventional power, speed and accuracy tradeoffs by using comparator excess with power gating abilities. This scheme used the little sized, ultra low power comparators. The power consumption is of 30mW with 1.2V.

S.Sheikhaei et al. [14] proposed a high velocity differential timed comparator circuit. This comparator contains a preamplifier and a latch followed by a dynamic latch that works as output sampler which contains of a full transmission gate and two inverters. The technology used is 0.35um and the resolution is 16mV for a 1V data signal reach with 3.3V supply. This technique consumes very low power of 2mW.

Bui Van Hieu, Seunghwar Choi et at. [9] Proposed new approach which coordinates a bubble error identification circuits and it can diminish all types of bubble error when contrasted with the past methodologies and the main advantage is that it expends low power. This method has great structure, very high speed and little chip area when contrasted with different structure. With the help of this ROM based technique we can reduce the latency and power dissipation and can rectify both first and second order bubble error. This system just distinguishes all bubble errors as opposed to attempting to rectify bubble error, which still can't cover all errors. At whatever point bubble error happen, there is at least one violent move from 0 to 1 in the thermometer input code. By identifying the violent move bubble error can be uncovered. One two input AND gate distinguishes violent move of every input and afterward all outputs of AND gates are gathered to recognizes bubble errors. The disadvantage is that it obliges an extensive number of additional transistors when compared to error detection circuits.

Mustafijur Rahman, K.L.Baishnab et al. [11] proposed the system to change over thermometer code into binary code using ROM based decoder which suppresses metastability and bubble errors accordingly reducing power dissipation, area usage and decrease delay. This design dispenses with the requirement of gray to binary converter and ROM which is coded by gray code making circuit easier and delay which is connected with the extra NAND stage is completely removed.

Christoph Sandner, Martin Clara, Andreas Santner et al. [15] proposed a 6 bit flash ADC ,large analog bandwidth and low power in 0.13um CMOS copper technology with 1.2GSps. This ADC attains to a effective resolution bandwidth (ERBW) of 700 MHz when working at 1.2 GSps expends 160mW power and at 600 MSps accomplishes an ERBW of 600MHz with just 90mW power consumption from 1.5V supply. The chip area is $0.12mm^2$ and requirement for reference resistor step, implicit sample and hold operation, no edge impacts in the interpolation network when contrasted with resistive addition and input capacitance is low of just 400fF and because of that we can safely drivable analog converter interface. This configuration demonstrates the efficiency of the capacitive interpolation construction modeling with distributed sample and hold for flash ADC in GHz range.

Mingzhen Wang and chien In Henry Chen et al. [13] proposed a 4 bit flash ADC with high spurious free dynamic for high data transmission correspondences using 130nm CMOS technology. They proposed timed digital comparator with dynamic offset concealment to enhance the ADC dynamic performance. This flash ADC has two and half clock cycle latency and low input capacitance is 300fF. The power consumption is 1.35mW with 1.2V with 2.5GHz conversion rate using a multistage pipelined design, this flash ADC enhances high sampling rate, low power, low input capacitance and there is no need of any reference resistor stage.

Panchal S.D., Dr. S.S.Gajre et al. [8] proposed pipelined 4 bit flash ADC using 0.18um CMOS technology to accomplish a high speed. The power, time and area are all minimized because the physical design is more conservative than other previous design and can be used for high speed ADC applications. This work concentrates on reducing the measure of analog design and circuitry in flash ADC.

## 4. Conclusion

In this paper we have examined different systems to design low power high speed flash ADC. Comparators and encoders are the two principle and vital parts of flash ADC. The comparator is a device for designing the mixed signal system and speed, area furthermore accuracy which is essentially characterized by its energy dispersal and speed is primary variables for high speed applications [7-8]. The encoder is a device that changes over the data starting with one arrangement then onto the next for the purpose of speed and compressions. After surveying the literature in details, we infer that the power utilization and speed assumes a vital part in the design of flash ADC. There are some advantages and disadvantages of the flash converter [11-12]. The focal point is its speed which takes next to no time to change over the analogue signal to the digital signal and the disadvantage is its cost and hardware requirements which consequences of the complexity of the circuit. In future, the fundamental concentrate on the work of the designing of the flash ADC is to execute a high speed with high exactness reduced size CMOS comparator

ISSN 2348 – 7968

and low offset comparator furthermore actualize the enhanced flash ADC with low power and high speed.

**Acknowledgment**

I would like to thank Dr. Manoj Nagmode for his constant guidance and encouragement.

## References

[1] Parthasarthy K.P. and Dr. K.C.Narasimhamurthy," A Low Power Comparator Design for 6-BitFlash ADC in 90-Nm CMOS," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 6, June 2014.

[2] K.Lokesh Krishna and T. Ramashri,"VLSI Design of 12-bit ADC with 1GSPS in 180nm CMOS integrating with SAR and two-step flash ADC,"Journal of Theoretical and Applied Information Technology, No. 1, Vol-68, 10 October 2014.

[3] Mamta Gurjar and Shyam Akashe,"Design Low Power Encoder for Threshold Inverter Quantization based Flash ADC Converter, "International Journal of VLSI design and Communication Systems (VLSICS), vol.4, No.2, April 2013.

[4] P.Rajeswari, Dr.A.R.Aswatha, Dr.R.Ramesh,"Performance analysis of flash analog to digital converter with track and hold circuit using CADENCE PSPICE,"IRACST-Engineering Science and Technology: An International Journal (ESTIJ), ISSN: 2250-3498, No.3, Vol.3, June 2013.

[5] Kirankumar Lad and M S Bhat,"A 1-V 1-GS/s 6-bit Low-Power Flash ADC in 90-nm CMOS with 15.75 mW Power Consumption, "In Computer Communication and Informatics (ICCCI), 2013 International Conference , IEEE, 2013.

[6] George Tom Varghese and K. K. Mahapatra,"A High Speed Low Power Encoder for 5 bit flash ADC,"IEEE, 2012.

[7] R.Komar, M. Bhat, and T. Laxminidhi, "A 0.5 v 300µw 50ms/s 180nm 6bit flash ADC using inverter based comparators," In Advances in Engineering, Science and Management (ICAESM), 2012 International Conference , pp. 331–335,IEEE, 2012.

[8] Panchal S. D., Dr. S. S. Gajre, Prof. V. P. Ghanwat," Design and implementation of 4-bit flash ADC using folding technique in cadence tool", International Journal of Advanced Research in Computer and Communication Engineering , ISSN : 2278 – 1021,Vol. 1, Issue 4, June 2012**.**

[9] Bui Van Hieu, Seunghwan Choi, Jongkug Seon, Youngcheol Oh, Chongdae Park, Jaehyoun Park, Hyunwook Kim, and Taikyeong Jeongt," A New Approach to Thermometer-to-Binary Encoder of Flash ADCs- Bubble Error Detection Circuit", IEEE MWSCAS, Aug 7- 10, 2011.

[10] Pradeep Kumar and Amit Kolhe," Design and Implemented of low power 3 bit flash ADC in 0.18 um CMOS,"International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, Volume-1, Issue-5, November 2011.

[11] Mustafijur Rahman, K. L. Baishnab, F. A. Talukdar," A Novel ROM Architecture for Reducing Bubble and Metastability Errors in High Speed Flash ADCs", International Conference, IEEE, 2010.

[12] T. Sundstrom and A. Alvandpour, "A 2.5-gs/s 30-mw 4-bit flash ADC in 90nm cmos,"In NORCHIP, 2008, pp. 264–267, IEEE, 2008.

[13] Mingzhen Wang and Chien-In Henry Chen," A High Spurious-Free Dynamic Range 4-bit ADC with Nyquist Signal Bandwidth for Wideband Communications", Instrumentation and Measurement Technology Conference (IMTC), Warsaw, Poland, May 1-3, IEEE, 2007.

[14] S.Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0.35 µm cmos comparator circuit for high-speed ADC applications," In ISCAS-2005. IEEE International Symposium on Circuits and Systems, pp. 6134–6137, IEEE, 2005.

[15] Christoph Sandner, Martin Clara, Andreas Santner, Thomas Hartig, Franz Kuttner," A 6bit, 1.2GSps Low-Power Flash-ADC in 0.13µm Digital CMOS", Proceedings of the Design, Automation and Test in Europe Conference and Exhibition, IEEE, 2005.

**Rahul Marotkar** has completed his B.E. in Electronics & Telecommunication Engineering from JIT Nagpur and currently pursuing his M.E in VLSI & Embedded System from MIT College Of Engineering, Pune and completing project using Tanner tool. His research interests include VLSI design and Digital Signal Processing.

**Dr.M.S.Nagmode** currently is Professor in E&TC department, MITCOE Pune. He is B. E. Electronics from VIT, Pune in the year 1996. He completed M.E. Electronics from Government College of Engineering, Pune in the year 1999. He received Ph. D. in E&TC from Government College of Engineering, Pune in the year 2009. His research interest is Signal Processing.