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Area and Delay efficient Multiplier using Vedic Mathematics

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Abstract

This paper proposes the design of an efficient 8×8 binary arithmetic multiplier by using Vedic Mathematics. A new methodology of Vedic Mathematics called as Urdhva-Tiryagbhyam sutra is used for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-select adder. From various addition techniques, carry select adder is being implemented for the addition of partial products because of the minimum delay obtained. A 4×4 Vedic Multiplier is designed using 9 –full adder and a special 4-bit adder which is having reduced delay. Then 8-bit multiplier is designed using four 4-bit multiplier and 3- carry select adders. The 8×8 Vedic Multiplier is coded in Verilog, synthesized and simulated using Xilinx ISE14.7 Software. Finally the objective of this paper is to optimize the multiplier circuit by using carry select adder instead of ripple carry adders. This reduces the delay to a great extent with minimal increase in hardware**.**

Keywords: *Vedic Mathematics, Urudhva-Tiryagbhyam algorithm, special adder, ripple carry adder, carry select adder.*

1. Introduction

Multipliers are key components of any high speed processors such as microprocessors, DSP processors, various FIR filters, etc. The performance of a system is generally determined by the performance of the multiplier because normally the multiplier is the slowest element in the system. Since multiplication dominates the execution time of most DSP applications, there is need of high speed multiplier. Hence increasing the speed and optimizing area of the multiplier is a major design issue. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. Thus this paper introduces a new method of multiplier design using carry select adder instead of other addition techniques.

1.1 Vedic mathematics

The word 'Vedic' is derived from the word 'Veda' which means the store-house of knowledge. It is a gift given by the ancient sages of India to the world. This refers to a technique of calculations based on a set of 16 sutras as algorithms. In which every individual can develop their own methods to do the calculations when compared with the modern mathematics.

1.2 Urdhva-tiryakbyham sutra

Urdhva-Tiryakbhyam Sutra is a multiplication algorithm which is applicable to all cases of multiplication. It literally means “Vertically and crosswise” where the partial products are generated simultaneously which itself reduces delay and makes this method fast.

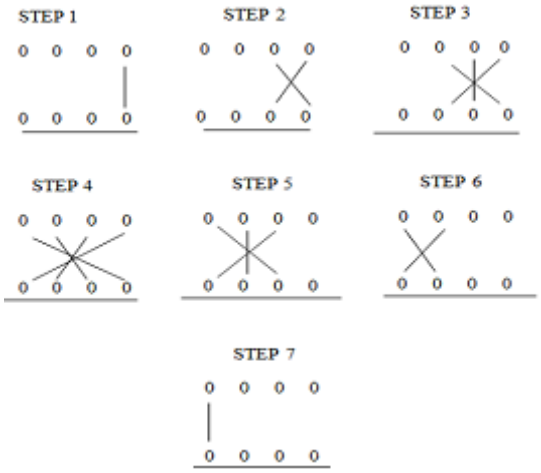

Figure 1: Line diagram of the multiplication

Consider two 4-bit binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. The partial products ($P_7P_6P_5P_4P_3P_2P_1P_0$) generated are given by the following equations:

i. $P_0 = a_0b_0$
ii. $P_1 = a_0b_1 + a_1b_0$
iii. $P_2 = a_0b_2 + a_1b_1 + a_2b_0 + P_1$
iv. $P_3 = a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0 + P_2$
v. $P_4 = a_1b_3 + a_2b_2 + a_3b_1 + P_3$
vi. $P_5 = a_1b_2 + a_2b_1 + P_4$
vii. $P_6 = a_3b_3 + P_5$
viii. $P_7 =$ *carry of* P_6

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2. Existing Design

(i) 4-Bit Multipliers The 4×4 Vedic multiplier is designed and is implemented using Verilog code. To reduce the delay of 4×4 multiplier, it is designed using a set of nine full adders and a 4-bit special adder.

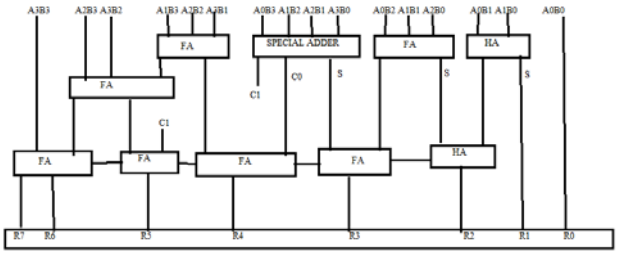

Figure 2: 4-bit Vedic multiplier

Special Adder in the 4*4 multiplier

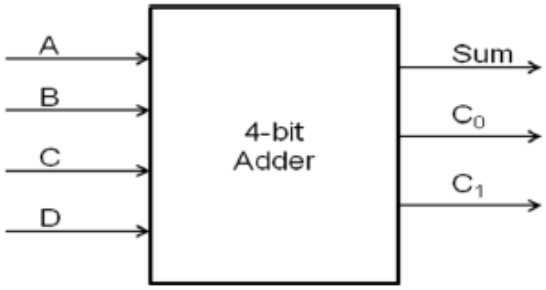

Figure 3: Structure of 4-Bit special adder.

The figure-3 shows the structure of the special adder used in the 4 bit vedic multiplier. Let A,B,C,D be the four inputs. C_0 and C_1 are LSB and MSB of carry outputs respectively and Sum is the sum of four inputs.

The Boolean expressions for the sum and carry are given below.

Sum= A XOR B XOR C XOR D
C_0 = ((NOT B) AND D) OR (C AND (NOT D)) OR (B AND (NOT C))
C_1 = A AND B AND C AND D

3. Proposed Design: 8-Bit Multiplier

The 8×8 Vedic multiplier in binary is designed and implemented using Verilog code. For reducing the delay of the multiplier, it is implemented using four Vedic 4*4 blocks and three carry select adders.

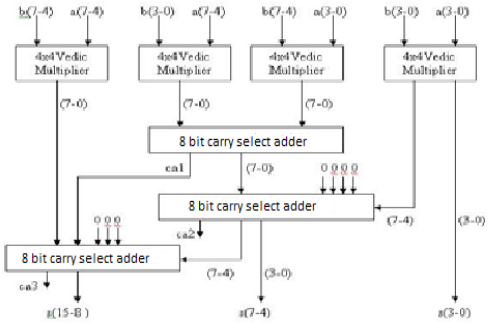

Figure.4 Architecture of 8×8 Vedic Multiplier

P=AxB=(AH-AL)x(BH-BL)
=AHxBH+(AHxBL+ALxBH)+ALxBL

Adder in the 8*8 multiplier: **Carry Select Adder**

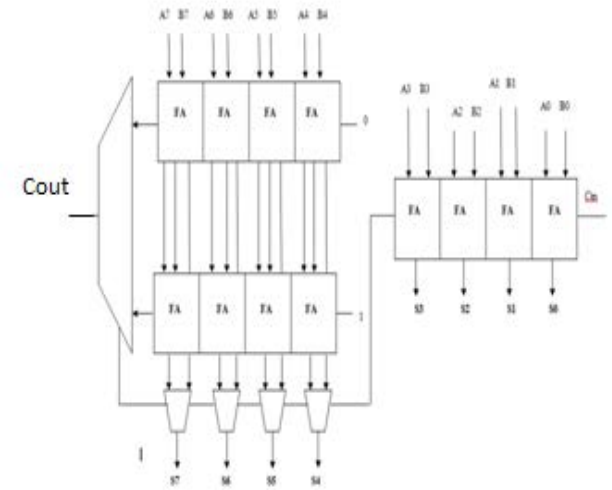

Figure.5 Structure of 8 bit Carry Select Adder

In the Carry select adder, the first four bits are added using normal ripple carry adder. The Carry select block is not used in the beginning of the computation for the first four

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bits. The most significant 4 bits are given to two 4-bit ripple carry adders which are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, the correct result is obtained using a MUX with the previous carry in as the bit selection input. The delay of this 8 bit adder will be four full adder delays, plus one MUX delay which is less than the eight full adder delays as in the case of 8 bit ripple carry adder. The result becomes more significant as the number of bits increases.

4. RESULT AND DISCUSSION

The proposed 8-bit multiplier is coded in Verilog HDL, simulated using Xilinx ISim simulator, synthesized using Xilinx XST for Spartan 7: xc7a100t-3csg324 FPGA and verified for all possible inputs. Inputs are generated using Verilog HDL test bench. The result is shown in unsigned decimal radix.

4.1 Simulation Output

The simulation result for 8-bit multiplier is shown in the Figure 6.

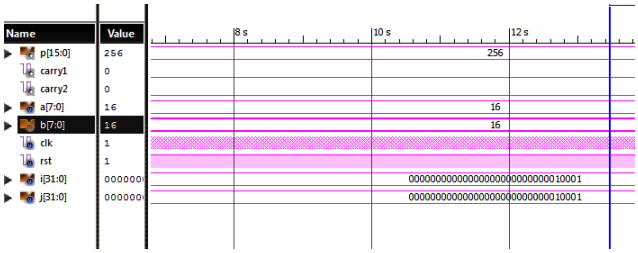

Figure.6 Simulation result of 8*8 Multiplier

4.2 Comparison with Existing Architecture

The 8-bit carry select adder designed is compared with the ripple carry adder in terms of total delay, LUTs, No. of slices used etc. The results obtained are tabulated in Table I. From table I, it is evident that there is a reduction in all the performance factors.

Table 1: Performance comparison of 8 bit Ripple carry adder with Carry select adder

	Ripple Carry Adder	Carry Select Adder
Slices	5	2
LUTs	8	4
IOBs	25	17
Delay	2.53ns	1.42ns

From table 1, it is clear that the delay has been reduced from 2.53ns to 1.42ns using the carry select adder.

The 8*8 multiplier is then designed using the carry select adder and is compared with the existing design using ripple carry adder and the results obtained are tabulated in Table 2.

Table 2: Performance comparison of 8*8 Multipliers

	Vedic Multiplier using Ripple Carry Adder [2]	Proposed Multiplier using Carry Select Adder
Slices	49	23
LUTs	111	46
IOBs	36	36
Delay	3.29ns	1.81ns

From table 2, the delay is found to be 1.81 ns, which is much less than the existing design delay of 3.29ns. Thus, it is clear that the proposed design outperforms the other popular multiplier architectures.

5. Conclusion

The proposed Vedic Multiplier circuit using Urdhva-Tiryakbhyam Sutra can be implemented in arithmetic and logical units of a DSP processor replacing the traditional designs. Generally the Vedic multipliers are much faster than the conventional multipliers. This gives us scheme for hierarchical multiplier design. So the design density gets condensed for inputs of large no of bits and the design gets augmented. This paper describes a method to effectively adjust the delay and power consumption for different multiplier structures using carry select addition technique. The work can further be extended to 16x16, 32x32 multipliers and their performance comparison can be studied. The proposed architecture can be used to develop

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a high speed complex number Multiplier with reduced delay.

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