

# Design and Implementation of Area Optimized Low Power Reversible Digital Multiplier

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## Abstract

Heat generation is the major drawback in conventional or irreversible electronic circuits or systems. In 1961, Rolf Landauer proved this drawback. But in 1973, Bennett gave the solution for this drawback. Bennett told that, there will be no or very less heat generation or energy dissipation, if the computation was reversible. So, the reversible logic is a solution for this drawback. Reversible logic can avoid the problem of heat generation, improve the system performance. This paper proposed an area optimized low power reversible digital multiplier. It was implemented in Xilinx-Spartan6 FPGA board and designed in SYMICA DE tool with final results.

**Keywords:** *Baugh-Wooley Approach, Complementary Pass Transistor Logic, Standard Reversible Logic Gates, Wallace Signed Multiplication.*

## 1. Introduction

Almost all the millions of gates used to perform logical operations in a conventional computer are irreversible. That is, every time a logical operation is performed some information about the input is erased or lost and is dissipated as heat. Reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. In 1961, Rolf Landauer [1] proves that, in conventional logic, gate operations will lead to energy dissipation regardless of technology. Exactly,  $kT \ln 2$  joules of energy will dissipate due to each lost bit of information.  $k$  is the Boltzmann's constant;  $T$  is the absolute temperature at which computation is performed. In 1973, Bennett [2] proved that  $kT \ln 2$  joules of energy dissipation would not occur if the

computation were carried out in a reversible manner. Reversible logic naturally takes care of heating because it implements only the functions that have one to one mapping between its inputs and outputs. Reversible logic gate can produce zero power dissipation under ideal conditions. This paper presented a reversible Wallace signed multiplier through modified Baugh-Wooley approach using standard reversible logic gates based on complementary pass transistor logic. Authors implemented proposed circuit in Full custom ASIC and tested the design in 45nm CMOS [8] technology.

The Wallace [10] approach has been used to construct a circuit with less delay. Multiplier circuits are divided into two categories: unsigned and signed. Several approaches have been presented to multiply the signed numbers, such as 2's complement, Baugh-Wooley [12], and modified Baugh-Wooley methods. In modified Baugh-Wooley method, the number quantity is considered as 2's complement.

## 2. Reversible Logic

### 2.1 Reversible Logic

A gate is reversible if there is a distinct output assignment for each distinct input. Thus, a reversible gate inputs can be uniquely determined from its outputs. A reversible logic [9] gate must have the same number of inputs and outputs.

### 2.2 Reversible vs Ir-reversible Logic, Standard Reversible Logic Gates

Conventional logic gates are irreversible. In reversible logic the number of inputs & outputs of a gate are equal,

where as in conventional logic they are not equal. Fanout is not possible in reversible logic. In reversible logic to achieve reversibility constant inputs & garbage outputs are necessary. In reversible logic, we can achieve output both in forward & reverse paths i.e. we can compute and uncompute the results. Feedback paths are not allowed in reversible logic. Reversible NOT, Feynman gates are called basic reversible gates. Feynman gate is also called CNOT gate. Authors used three standard reversible logic gates to construct proposed multiplier. They are toffoli [3],[4] gate(TG), peres[5] gate(PG), haghparast navi[6],[7] gate(HNG). TG, PG are 3\*3, HNG is 4\*4 gate. PG is one through, TG and HNG are two through gates. TG is a universal reversible logic gate. Two peres gates can be combined to form a full adder.

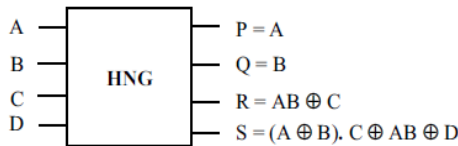


Fig. 1 Symbol of HNG Gate.

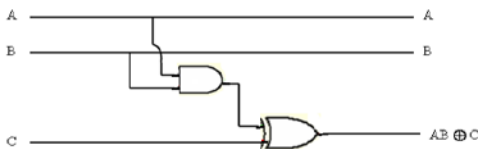


Fig. 2 Logic Diagram of Toffoli Gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 3 Truth Table of Peres Gate.

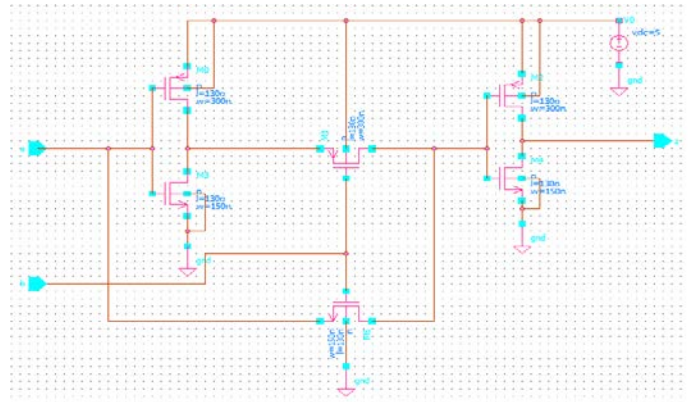


Fig. 4 Xor Gate Schematic in Symica.

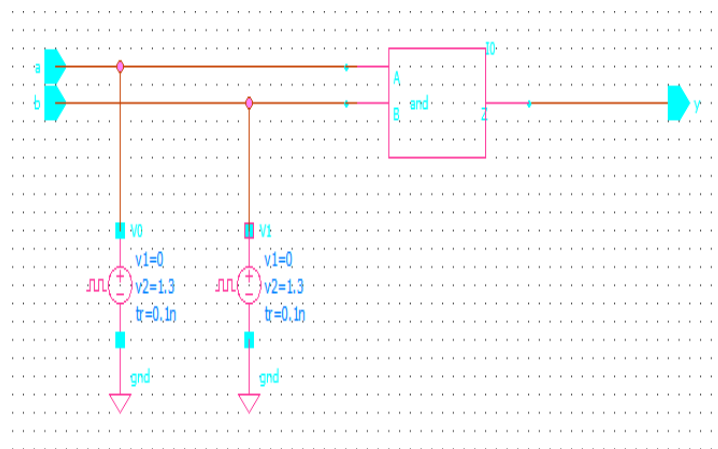


Fig.5 Test Bench of AND Gate in Symica.

### 3. Proposed Reversible Multiplier and Results

Proposed reversible multiplier is 5-bit. Authors denoted inputs of multiplier as A, B. A=10101, B=01010 and the multiplication result is 1110010010. Here, input and output values are in 2's complement. Fig. 6 shows partial product generation and addition, fig.7 shows overall multiplication, fig.8 shows Xilinx Isim simulator output and fig.9 shows symica waveforms. For the proposed circuit 10 garbage outputs, 21 constant inputs, 1 NOT gate are required. For partial product generation 25 TG gates are required. For partial product addition 4 PG gates, 16 HNG gates are required. Garbage output refers to the number of outputs which are not used in the synthesis of a given function. These are very essential without this reversibility cannot be achieved. Constant inputs refer to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

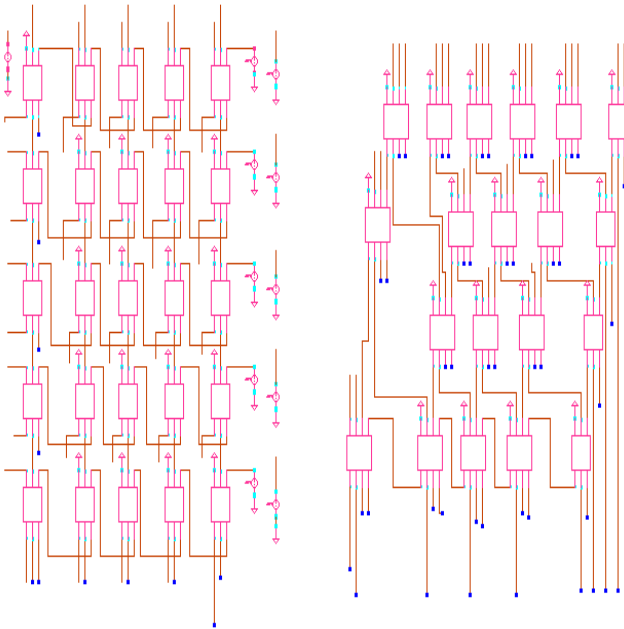


Fig. 6 Partial Product Generation and Addition.

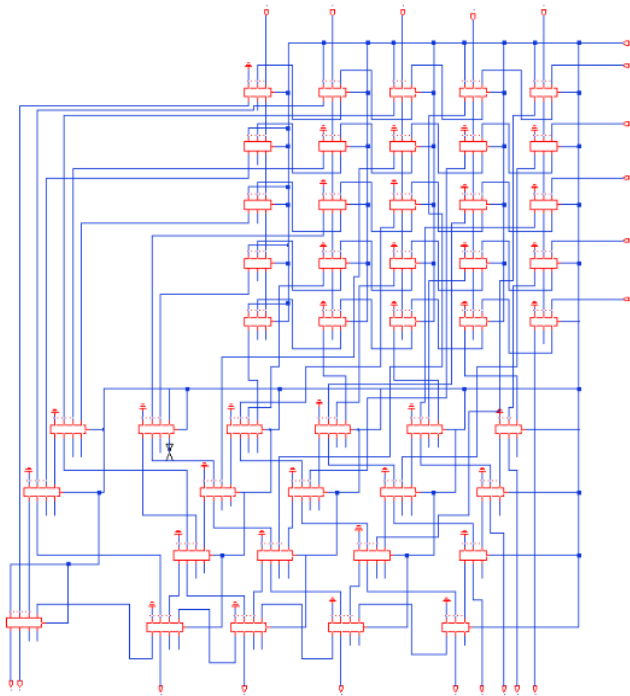


Fig. 7 Overall Multiplication.

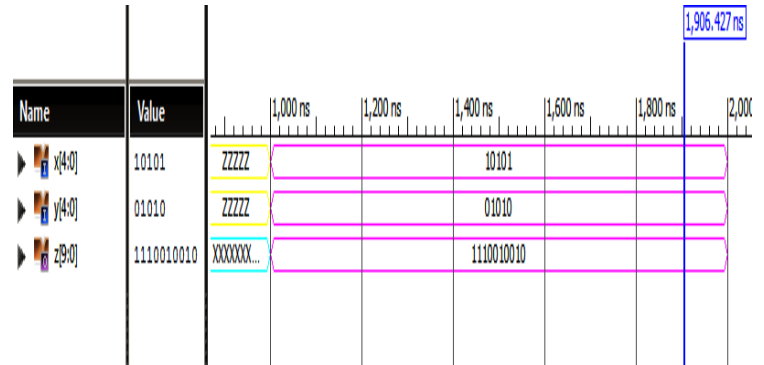


Fig. 8 Xilinx Isim Simulator Output.

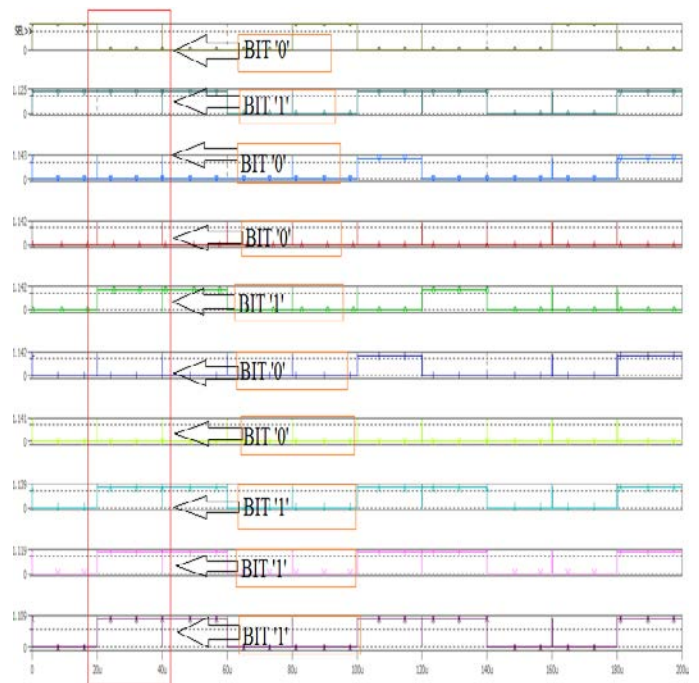


Fig. 9 Symica Waveforms.

Fig.10 shows power requirement. Table I shows the power requirement comparison and Table II shows the transistor requirement comparison. Power requirement of existed multiplier[13] with 45nm technology is  $6\mu w$ , where as in proposed multiplier with 45nm technology it is  $5\mu w$ . Transistor requirement of existed multiplier[13] is 912, where as in proposed multiplier it is 818.

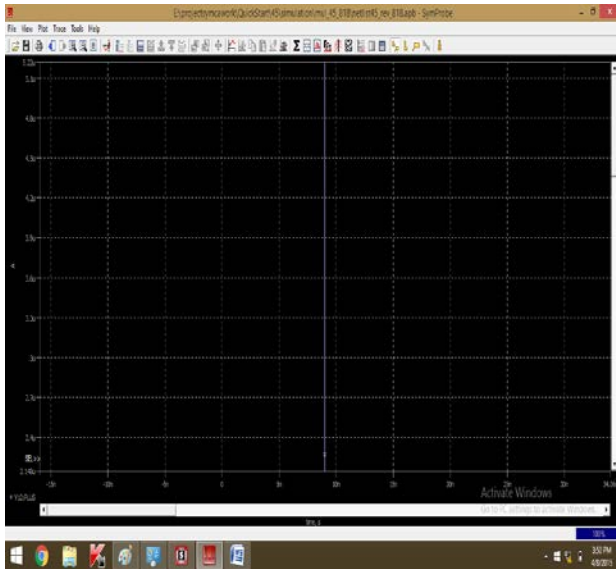


Fig. 10 power Requirement.

Table 1: Power Requirement Comparison

Technology Used	Power Consumed
(Ir-reversible Multiplier)0.5 $\mu$ m	6mw
(Existed Multiplier)0.5 $\mu$ m[3]	4mw
(Existed Multiplier)45nm[4]	6 $\mu$ w
(Proposed Multiplier)45nm	5 $\mu$ w

Table 2: Transistor Requirement Comparison

Type of the multiplier	Transistors required
Ir-reversible multiplier (5x5)	810
Existed multiplier[12] (5x5)	1264
Existed multiplier[13] (5x5)	912
Proposed multiplier (5x5)	818

#### 4. Conclusions

The main advantage of reversible logic is low power dissipation .Reversible logic has many applications such as low power CMOS,Nano technology, quantum computing, optical information processing, DNA computing, bioinformation, laptop, handheld and wearable computers etc. By using this reversible logic concept,so

many authors developed some standard reversible logic gates or circuits,which are useful to design and implement reversible logic systems.Multiplier is the one of it's kind & it is the most useful digital circuit or system.In fact, every computational system needs multiplier.So far,so many authors proposed various reversible multiplier circuits.In 2014,Hatkar A.P & Hatkar A.A proposed "ASIC design of reversible multiplier circuit"[12].And in 2015,K.Pradeep and team proposed "Design and implementation of H/W efficient Multiplier: Reversible logic gate approach"[13]. This paper, successfully implemented and designed an area optimized low power reversible digital multiplier,and proved that it was a power & hardware efficient multiplier when compared to existed multipliers[12][13].

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