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Investigation of the effect for 32nm NMOS Transistor and Optimizing Using Taguchi Method

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Abstract- **This paper describes our investigation of the effect of seven processes' parameters on threshold voltage (V_{TH}) in the fabrication of a 32nm NMOS transistor. The parameters are HALO implantation, S/D Implantation, Compensation implantations, SiO_2 thickness, V_{TH} adjustment implantation, polysilicon thickness and silicide annealing time. The setting of process parameters were determined by Taguchi method L_{18} experimental design. From there, the level of importance of each of the process parameters on threshold voltage was determined using analysis of variance (ANOVA). Transistor fabrication was performed by using Silvaco ATHENA module. Silvaco ATLAS module takes care of electrical characterization for the device. These two simulators results were analyzed with Taguchi method to aid in design and optimizing process parameters. Threshold voltage (V_{TH}) results were used as the evaluation parameters. The results show that the V_{TH} value 0.10315 V for NMOS can be achieved respectively, much closer to the ITRS prediction than our previous L9 experiment result. As the conclusion, by utilizing L18 Taguchi Method shown that process parameters can adjust threshold voltage (V_{TH}) to a stable value of 0.10315 V that is well within ITRS prediction for 32nm transistor.**

Keywords: *Silicon MOSFET 32nm, Taguchi L_{18}, HALO, Compensation Implantation, S/D implantation, Threshold voltage, Taguchi Method*

INTRODUCTION

CMOS downscaling is one of the fastest moving technologies since mid 70s [1]. Modernization of human lifestyle in simplifying and improving their life aspects has been the driving factor of this advancement. Following Moore's law, the number of transistor per silicon area doubled every 18 months [1], with wider use of mobile applications and portable equipments has further lead to reducing the area available to put the transistors. The increasing wafer fabrication process parameter variation has been perceived as one of the major roadblocks to further technology scaling.[7] Threshold voltage mismatch is one of the main analogue performance indicators of a CMOS technology, since it determines the accuracy-speed-power trade-off of the basic analogue building blocks. The fundamentally lower level threshold voltage mismatch is largely due to doping fluctuations [7-9]. It is resulting in complications to get the right threshold voltage (V_{TH}) value for the transistor and also to control the gate leakage current to an acceptable level. Reaching 32nm, we are almost at the silicon oxide gate atomic resolution and at this juncture, it is widely believed and proved that high-K metal dielectric will start to replace the traditional silicon oxide (SiO2)[8]. Hafnium and Zirconium are the two most popular metals under consideration. However, replacing the silicon dioxide gate dielectric with another material adds complexity to the manufacturing process and that is why we try to explore the possibility of staying with SiO2. In doing so we study the effect of four parameters that are widely being used in CMOS wafer fabrication before high-K metal dielectric being introduced and try to optimize the value or level used for each of them in order to produce a working transistor. The seven fabrication factors that were selected are S/D Implantation, Compensation implantations, SiO2 thickness, V_{TH} adjustment implantation, polysilicon thickness and silicide annealing time. Taguchi method is used as an experimental method in finding an optimum solution for the four factors.

In our experiment, S/D implantation is being done with Arsenic followed by phosphor for NMOS. Getting the right dosage would be very important to ensure a transistor works perfectly as a switch in our digital device world. In NMOS, halo implantation is done by having P-type impurities implanted to the desired depth in the semiconductor substrate prior to forming N-channel lightly doped source/drain areas. Subsequently, moderately or heavily doped source/drain regions are formed, followed by activation annealing. The halo implants diffuse to form halo structures at the desired location, thereby reducing short channel effects, such as subsurface punch-through. Figure 1 shows the effect of V_{TH} values as we scale down with and without halo implantation.

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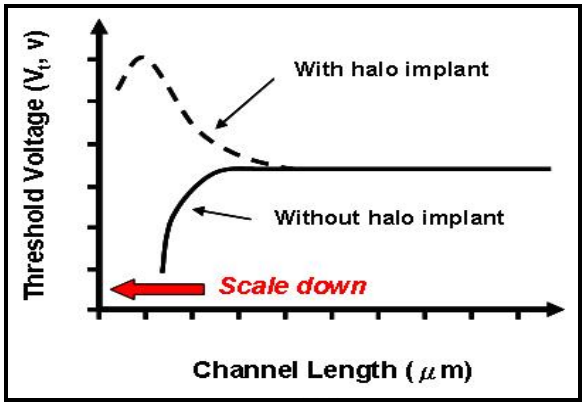

Figure 1 - Effect of Halo Implantation to V_{TH} values in CMOS Downscaling [5]

Compensation implantation is performed to minimize transistor side capacitance. This is very important to reduce delay time and to ensure that a transistor gives the expected high performance speed it guarantees. In CMOS, phosphorous is used as impurity for this purpose for NMOS [6]. The fourth factor is SiO2 thickness. The thickness is varied in three levels to be used with other parameters. As mentioned before, as SiO2 becoming thinner, electrons are more likely to punch through the oxide layer from gate to the channel and add to the current there. This can even result in the transistor being turned-ON even when VG < V_{TH}. As such it is critical to get the right SiO2 thickness for a working CMOS transistor. V_{TH} adjustment implantation is being done with implanting Boron difluoride (bf2) for NMOS. The next factor is polysilicon thickness. Polysilicon is a crystal silicon structure that unlke silicon, will allow conduction. This structure on top of SiO2 is important in ensuring that charge are quickly transferred and stored at the gate, acting as the transistor switch. The final factor is the annealing time for self-aligned metal silicide technology. This silicide has been widely used to reduce resistance of polysilicon gates.Metal silicides such as titanium silicide (TiSi2), tungsten salicide (WSi2), cobalt salicide (CoSi2) and nickel salicide (NiSi2) are widely used for this purpose. These metals react with polysilicon, to form metal silicide layer that possesses better physical and electrical properties to interface with aluminium. The silicide need to be optimally annealed in order to obtain a good ratio of metal silicide to silicon in the gate structure.

Taguchi Method is applied in order to achieve an optimum solution with minimal number of experiments performed. In semiconductor industry, actual fabrication is extremely expensive and time consuming, with the complexities exponentiation as we reach nanometer regime. The robust nature of Taguchi enables us to reduce project duration by varying the factors at three different levels and running only eighteen sets of experiment (per L18 orthogonal array) as suggested by Taguchi. By analyzing the result accordingly, we are able to predict the optimum fabrication recipe in producing a 32nm NMOS transistor with the V_{TH} value of 0.1099 V and the values is well within ITRS prediction for 32nm transistor [9].

Experiment Description

The experiment starts with fabricating a 32nm NMOS transistor. We fabricate a transistor based on one as done in previous experiments by [Mohamad et. al.]. The first step is to initiate a silicon bulk, with crystal orientation of 100. Next we perform an oxidation of the top layer using dry oxygen, on a temperature of 970ºC for 20 minutes. The resulting oxide layer is used as a mask for the P-well implantation process, which is the next step. For this, boron is used with a dose of 3.75x1012 ions/cm2 with implantation energy of 100eV, with the ion gun being tilted 7º. The silicon bulk will then be diffused in nitrogen for 30 minutes and dry oxygen for 36 minutes in order to ensure boron molecules being separated nicely in the bulk. The masking oxide is then etched and the following step is to produce Shallow Trench Isolator (STI). The bulk is diffused to dry oxygen for 25minutes at 900ºC to grow a pad oxide layer. Next, a 1500Å nitride layer is deposited followed by a photoresist deposition with a thickness of 1.0µm. Then, the photoresist and the nitride will be etched at the top of STI area followed by trenching process on the silicon bulk. The trench wall passivation will follow by diffusing the surface to a 900ºC. Next, a sacrificial oxide layer is grown and etched followed by a sacrificial nitride layer. This will allow the trench to be completed. Modification starts when we reach the gate oxide fabrication process. At this point, we got a silicon substrate doped with boron of concentration 3.75x1012ions/cm2, also with implantation energy of 100eV and being tilted 7º, to create a p-well. Then, we grow the sacrifial oxide layer by diffusing the silicon subrate surface for 45 minutes, at 900ºC, with dry oxygen environment at 1.0 a.t.m. We then use extract command to get the sacrificial oxide thickness at the coordinate x=0.1 of the transistor. To introduce a process noise (N1), in a second run of the device fabrication simulation, we change the diffusion temperature to 901ºC. Next process is to grow the gate oxide. To do this, the silicon bulk is diffused with dry oxygen, at 825ºC, at 1.0 a.t.m. for short time. The short time is needed to ensure a thin, no more 1.1nm of oxide thickness is grown. After the gate is built, the next step is to implant boron difluoride (bf2) at the well active area in order to adjust V_{TH} value. The dosage is about 1.75x1011ions/cm2 with relatively low implantation energy of 5eV while also being tilted 7º. Polysilicon will then be deposited on the top of the bulk and etch accordingly to produce the gate contact point as desired. Later on, halo implantation will take place with dose of 1.28.x1013ions/cm2, 160eV implantation energy while being tilted 30º. Nitride layer will then deposited on top of the structure and immediately etched to expose the top of silicon layer. Then spacers are grown at each of the polysilicon sides followed by implanting

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the two N++ regions. To create the source and drain, firstly arsenic with dose of 5.00x1013ions/cm2, 12eV implantation energy of while being tilted 7ºc is implanted first followed by phosphor with dose of 1.5.x1012ions/cm2, 100eV implantation energy while being tilted 7ºc.

The next step is creating an oxide mask on the top of polysilicon gate in order to create silicide structure on the top of the gate. Cobalt will then be deposited to on the top of the structure and then be annealed in nitrogen environment. This will allow cobalt to penetrate into polisilicon producing ohmic contact structure. Afterwards, the unused cobalt is etched away. The introduction of the second noise happens at the next step, where we anneal the structure for 6 seconds, on a temperature of 910ºC, nitrogen environment at 1 a.t.m. The noise (N2) is introduce by reducing the anneal temperature to 909ºC. This annealing process is to deepen the cobalt molecules into the polysilicon. The next process is to prepare source and drain masking, first for Compensation implant with dose of 3.7.x1013ions/cm2, 60eV implantation energy and being tilted 7ºc, and then followed by aluminum contact deposition. This is followed by 25 minutes annealing at 850ºC. Next aluminum layer is layered on the top of the structured and then etch accordingly to form the metal contact to source and drain. At this point the transistor is completed. Then, the completed transistor will undergo electrical characteristic simulation to find the leakage current.

Taguchi Orthogonal L18 Array Method

The two noise factors will create four set of experiments consisting of 72 runs. A four set of L18 orthogonal array runs, is the minimum number of results needed for our project Taguchi analysis. The values of the process parameter and noise factor at the different levels are listed in Table 1 and Table 2 respectively.

Table 1 – Process Parameters and their Levels

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implantation	atom/cm^3	1.29x10^{13}	1.28x10^{13}	-
B	S/D Implantation	atom/cm^3	5.2x10^{13}	5.0x 0^{13}	4.8x10^{13}
C	Compensation Implantation	atom/cm^3	3.8x 10^{13}	3.7 x 10^{13}	3.6 x 10^{13}
D	Silicide Anneal Temperature	ºC	880	900	920
E	Oxide Thickness	nm	1.1	1.2	1.3
F	Vth Adjustment Implantation	atom/cm^3	1.70 x 10^{11}	1.75 x 10^{11}	1.80 x 10^{11}
G	Poly Thickness	nm	6.72	7.72	8.72
H	empty	-	-	-	-

Table 2 – Noise Factors and their Levels

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide layer	oC	900 (X1)	902 (X2)
Y	Cobalt annealing	oC	908 (Y1)	910 (Y2)

In this research, an L18 ($2^1 3^7$) orthogonal array which has 18 experiments was used. The experimental layout for the process parameters using the L18 ($2^1 3^7$) orthogonal array is shown in Table 3.

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Table 3 – Experimental Layout Using L18 ($2^1 3^7$) Orthogonal Array

Exp. No.	Process Parameter level							
	A	B	C	D	E	F	G	H
1	1	1	1	1	1	1	1	1
2	1	1	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3
4	1	2	1	1	2	2	3	3
5	1	2	2	2	3	3	1	1
6	1	2	3	3	1	1	2	2
7	1	3	1	2	1	3	2	3
8	1	3	2	3	2	1	3	1
9	1	3	3	1	3	2	1	2
10	2	1	1	3	3	2	2	1
11	2	1	2	1	1	3	3	2
12	2	1	3	2	2	1	1	3
13	2	2	1	2	3	1	3	2
14	2	2	2	3	1	2	1	3
15	2	2	3	1	2	3	2	1
16	2	3	1	3	2	3	1	2
17	2	3	2	1	3	1	2	3
18	2	3	3	2	1	2	3	1

Result and Discussion

The results of threshold voltage (V_{TH}) were analyzed and processed with Taguchi Method to get the optimal design. The optimized results from Taguchi Method were simulated in order to verify the predicted optimal design.

Analysis for 32nm NMOS Device

The experimental results for threshold voltage for NMOS device is shown in Table 4.

Table 4 – V_{TH} Values for NMOS Device

Exp. No	Threshold Voltage (Volts)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	0,083112	0,08253	0,09109	0,0815494
2	0,112537	0,115241	0,12165	0,111411
3	0,130924	0,128656	0,13891	0,128436
4	0,108381	0,107947	0,11271	0,107461
5	0,15116	0,149648	0,1572	0,148439
6	0,110235	0,109768	0,11086	0,109123
7	0,131046	0,129758	0,13914	0,129111
8	0,099418	0,097856	0,10749	0,092365
9	0,089261	0,0887469	0,09358	0,083763
10	0,13762	0,131387	0,14113	0,129934
11	0,110658	0,110147	0,11097	0,110083
12	0,120117	0,117148	0,12107	0,112527
13	0,079926	0,074863	0,08276	0,071034
14	0,140311	0,137954	0,14081	0,133875
15	0,110214	0,110025	0,11078	0,109956
16	0,111831	0,11074	0,11229	0,11014
17	0,120037	0,118674	0,12075	0,115381
18	0,091473	0,091034	0,09638	0,089896

In this research, threshold voltage of the 32nm devices belongs to the nominal-the-best quality characteristics. The S/N Ratio, η can be expressed as:

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

While n is number of tests, μ is mean and σ is variance. By applying Equations (1), the η for each device were calculated and given in Table 5.

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Table 5 – Mean, Variance and S/N Ratios for NMOS Device

Ex. No.	A	B	C	D	E	F	G	empty	Mean	Variance	S/N Ratio (Mean)	S/N Ratio (Nominal-the-Best)
1	1	1	1	1	1	1	1	1	8,46E-02	1,93E-05	-21,46	25,69
2	1	1	2	2	2	2	2	2	1,15E-01	2,10E-05	-18,77	28,00
3	1	1	3	3	3	3	3	3	1,32E-01	2,42E-05	-17,61	28,56
4	1	2	1	1	2	2	3	3	1,09E-01	5,85E-06	-19,24	33,08
5	1	2	2	2	3	3	1	1	1,52E-01	1,51E-05	-16,39	31,82
6	1	2	3	3	1	1	2	2	1,10E-01	5,39E-07	-19,17	43,51
7	1	3	1	2	1	3	2	3	1,32E-01	2,17E-05	-17,57	29,07
8	1	3	2	3	2	1	3	1	9,93E-02	3,91E-05	-20,06	24,02
9	1	3	3	1	3	2	1	2	8,88E-02	1,61E-05	-21,03	26,89
10	2	1	1	3	3	2	2	1	1,35E-01	2,77E-05	-17,39	28,18
11	**2**	1	**2**	**1**	**1**	**3**	**3**	2	1,10E-01	1,80E-07	-19,14	48,32
12	2	1	3	2	2	1	1	3	1,18E-01	1,48E-05	-18,58	29,73
13	2	2	1	2	3	1	3	2	7,71E-02	2,73E-05	-22,25	23,39
14	2	2	2	3	1	2	1	3	1,38E-01	1,00E-05	-17,19	32,81
15	**2**	2	**3**	**1**	**2**	**3**	**2**	1	1,10E-01	1,40E-07	-19,15	49,40
16	2	3	1	3	2	3	1	2	1,11E-01	9,70E-07	-19,07	41,06
17	2	3	2	1	3	1	2	3	1,19E-01	5,67E-06	-18,51	33,95
18	2	3	3	2	1	2	3	1	9,22E-02	8,22E-06	-20,71	30,14

Referring to Table 5, S/N Ratios for the rows 6, 11, 15 and 16 have 43.51dB, 48.32dB, 49.40dB and 41.06dB respectively. This result implies that the process parameter combinations give the best insensitivity for the response characteristic. The effect of each process parameter on the S/N ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio for each level of the process parameters are summarized in Table 6. In addition, the total mean of the S/N ratio for the 9 experiments are also calculated and listed in Table 6.

Table 6 – S/N Ratio for the Threshold Voltage

Symbol	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N	Max - Min
		Level 1	Level 2	Level 3		
A	Halo Implantation	30,07	35,22		32.65	
B	S/D Implantation	31,41	35,67	30,86		
C	Compensation Implantation	30,08	33,15	34,70		
D	Silicide Anneal Temperature	36,22	28,69	33,02		
E	Oxide Thickness	34,92	34,21	28,80		
F	Vth Adjustment Implantation	30,05	29,85	38,04		
G	Poly Thickness	31,33	35,35	31,25		
H	Empty	31,54	35,19	31,20		

Figure 1 shows the factor effect plots for (i) S/N Ratio (purple or magenta color) and (ii) Mean (light green color) for NMOS device. The dashed line is the values of the overall- mean of the S/N ratio and Mean respectively. Basically, the larger S/N ratio, the better quality characteristic for the threshold voltage.

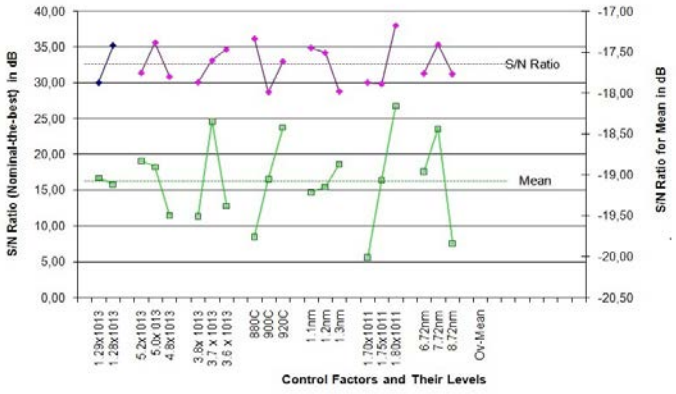

Figure 1 – S/N graph for threshold voltage in NMOS Device

(NOTE: we will remove the plot for the "empty" column and change Y-2 axis title to "Mean in dB")

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Analysis of Variance (ANOVA)

For 32nm NMOS Devices

The priority of the process parameters with respect to the V_{TH} was investigated to determine more accurately the optimum combinations of the process parameters. The result of ANOVA for the NMOS device is presented in Tables 9. The percent factor effect on S/N Ratio indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution will have a greater influence on the stability of V_{TH} with respect to the noise parameters.

Table 7 – Result of ANOVA for NMOS Device

Symbol	Process Parameter	Degree of Freedom	Sum of Square	Mean square	Factor Effect on S/N Ratio (%)	Factor Effect on Mean (%)
A	Halo Implantation	1	119	119	11	0
B	S/D Implantation	2	83	42	8	4
C	Compensation Implantation	2	67	33	6	12
D	Silicide Anneal Temperature	2	171	86	16.4	13
E	Oxide Thickness	2	135	67	13	1
F	Vth Adjustment Implantation	2	262	131	25	25
G	Poly Thickness	2	66	33	6	14
H	Empty	0	0	0	-	-

The results clearly show that the V_{TH} adjustment implantation (25%) has the most dominant impact to the S/N Ratio of the threshold voltage in NMOS device, whereas silicide anneal temperature was the second ranking factor (16.4%). These are called dominant factors. The percent effects of oxide thickness, halo implantation and S/D Implantation on S/N ratio are lower being 13%, 11% and 8% respectively. These are called significant factors. The percent effects of Compensation implantation and poly thickness on S/N ratio are much lower being 6% and 6% respectively. The best settings of dominant and significant factors can be found from the factor effect plots and Analysis of Mean (ANOM) and these are: A2B2D1E1F3. Because factors C and G were found to have insignificant or negligible effect, both of them can be pooled and they can be set at any level. Furthermore, one of the factors C and G is likely to be a good candidate to act as "adjustment factors" as their effect on S/N ratio is negligible. The suitable levels for adjustment for C appear to be between C2 and C3 and for G these appear to be between G2 and G3. The full recommendation for confirmation experiment is to perform 4 simulations for factorial combinations of C2, C3 and G2,G3 (C2G2, C2G3, C3G2, C3G3) keeping all other factors at their best settings A2,B1,(C2 or C3),D1,E1,F3,(G2 or G3). The aim of these 4 simulations will be (i) to get S/N ratio > 49.40 (this being the highest in 18 experiments) and (ii) simultaneously put the value of V_{TH} on target value of 0.110V.

NOTE: V_{TH} =0.110V has been achieved with S/N ratio of 53dB
→ Which is more than the best-of-18 value of 49.4 dB?)

Confirmation of Optimum Run

With all information, it can be clearly said that for the design, either Compensation implantation or poly thickness can be defined as an adjustment factor because it has a small effect on the S/N Ratio (variance) and large effect on the mean. In NMOS device, the value of Compensation implantation or poly thickness can be adjusted. The adjustments have to be done to get the threshold voltage closer to the nominal value or target value. The best setting of the process parameters for the device which had been suggested by Taguchi method are shown in Table 8.

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Table 8 – Best Setting of the Process Parameters

Symbol	Process Parameter		Unit	Best Value	
A	Halo Implantation	A2	atom/cm^3	1.28x10^{13}	
B	S/D Implantation	B1	atom/cm^3	5.2x10^{13}	
C	Compensation Implantation	C2	atom/cm^3	3.7 x 10^{13}	CONTROL FACTOR WE WILL SWEEP FROM 3.6 x 10^{13} TO 3.7 x 10^{13}
D	Silicide Anneal Temperature	D1	^{o}C	880	
E	Oxide Thickness	E1	nm	1.1	
F	Vth Adjustment Implantation	F3	atom/cm^3	1.80 x 10^{11}	
G	Poly Thickness	G3	nm	8.72	
H	Empty	HN	-	-	

From the above parameters as shown in Table 8, the final simulation was performed to verify the accuracy of the Taguchi Method prediction.

The value of Compensation Implantation was adjusted within 3.6 x 10^{13} TO 3.7 x 10^{13} until the value of threshold voltage (V_{TH}) closer to 0.11v. By doing the value sweep, the Compensation Implantation doping as the optimum solution for fabricating a 32nm NMOS transistor is 3.63 x 10^{13} atom/cm3. By adding noise factors to this simulation and run them we get the result as follow

Table 9 – Results of Further Runs of Confirmation

Experiment with Added Noises

Device	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
NMOS	0.10997 v	0.10963 v	0.11008 v	0.10959 v

From the above results of further runs of confirmation experiment with added noises as shown in Table 9 For NMOS, the mean is 0.1099 v with s/n ratio of 53 db. The values are well within the target set by ITRS.

Conclusion

Since threshold voltage (V_{TH}) is taken as nominal the best the effects of various parameters on S/N ratio and adjustment parameter " Compensation Implant " for NMOS threshold voltage (V_{TH}), because this have large effect on the mean of threshold voltage (V_{TH}) but little effect on variance of threshold voltage (V_{TH}) .

This experiment proves that Taguchi Analysis can be effectively used in finding the optimum solution in producing 32nm CMOS transistor. At this technology juncture, we still manage to find a working transistor with threshold voltage and leakage current well within International Technology Roadmap for Semiconductor (ITRS) prediction. In this research, the main finding is that, ironically, "V_{TH} Adjustment Implantation" can NOT be used as V_{TH} adjustment parameter, but "Compensation implant" can be used for adjusting V_{TH} on to its target value of 0.110 V.

References

[1] Taur, Y., Mii, Y.J., Wong, D. J., Buchanan, D. A., Wind, S. J., Sai-Halasz, G. A. & Nowak, E. J. (1995). CMOS Scalling into the 21st Century: 0.1µm and Beyond. IBM J.Res.

[2] Toshihiro Sugii, Kiyoshi Watanabe & Shinji Sugatani. (2003). Transistor Design for 90nm Generation and Beyond. Fujitsu Science & Technology J. 39(1).

[3] Kazunari Ishimaru (2008). 45nm/32nm CMOS – challenge and Perspective. Toshiba America Electronic Component. Elsevier Journal

[4] Taib Ziad Mohamad, Ibrahim Ahmad, Azami Ibrahim (2006). Optimum Solution in Fabricating 65nm NMOS Transistor Using Taguchi Method. Universiti Kebangsaan Malaysia. WSEAS Conference. Development.39(112).

[5] Fang Y.K, Lai CM , Chiang Y.T,(2007) ,Evaluation Of Post-annealing-induced defect dynamic behaviors on 90nm In-halo n-MOSFETs with low frequency noise and charge pumping measuring techniques, IEEE ELECTRON DEVICE LETTERS,28(2), p.142-4.

[6] Curello G., Rengarajan R., Faul J., Kieslich A., Glawischnig H, (2000) Junction Capacitance Reduction by S/D Junction Compensation Implantation, IEEE Journal

[7] Liang-Teck Pang, Borivoje Nikolic, "Impact of Layout on 90nm Process Parameter Fluctuations",IEEE Symposium on VLSI circuit Digest of Tecnical papers", 2006

[8] Sleight JW, et al (2006). Challenges and opportunities for high performance 32nm CMOS technology. IEDM Tech Digital.

[9] < http://www.itrs.net>