An Optimum VLSI Design of a 32-Bit ALU

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ABSTRACT

The execution standards of every VLSI design are defined by few fundamental factors. Those factors can be logic delay, wattage and space occupied by microchip. Variety of system syntaxes are based on execution standards. All the mathematical transactions are performed by calculator. Adder component acts as calculator to perform mathematical transactions in an ALU. This project details 32-bit ALU VLSI architecture. Different set of configurations of adder are explored in detail. The configuration that meets the execution standard is used for ALU architecture. Lastly 32-bit ALU architecture is completed by making use of mixed logic techniques i.e CMOS technique is preferred to organize fundamental digital functions, pseudo NMOS technique is preferred to organize AND gate and pass transistor technique is preferred to organize multiplexers. ALU is organized and simulated in HDL (Model simulator). Further the code is loaded on FPGA Spartan 3E kits for real time realization.

Keywords: *VLSI-Very Large Scale Integration, CMOS-Complementary Metal Oxide Semiconductor, ALU-Arithmetic and Logic Unit, HDL-Hardware Description Language.*

1. Introduction

The most preferred module of a CPU is ALU which execute mathematical and digital transactions include adding two-binary inputs, subtracting two-binary inputs, multiplying and dividing two-binary numbers. Digital transaction includes, NOT, AND, OR, XOR, NAND, NOR and other user defined functions. Binary adder is a necessary sub-module in an ALU to perform mathematical transactions. Based on systematic way of forwarding carry bit, variety of binary adder configurations are present. Adder configurations are bounded due to space, velocity and power occupied by a microchip.

32-bit ALU evolves a lot of operation incorporating nearly all digital transaction and four mathematical transactions. Architecture of ALU is completed by clock-gating. This decreases occupied power of a microchip. Carry-bit is executed individually in advanced configurations for instant addition. Some advanced adders are Carry-look-ahead adder (CLA), carry-skip adder (CSKA) and carry-select-adder (CSA).Delay caused by forwarding carry-bit is expressed in detail at transistor background. Different techniques are compared in terms of velocity and delay, to execute variety of functions of ALU.

2. DESIGN METHODOLOGY

2.1 Transistor Techniques

2.1.1 CMOS Technology: NMOS technology was preferred to a great degree in the era of 80’s, whereas CMOS was still not completely developed. CMOS is composed of two transistors namely NMOS and PMOS. Recently CMOS technology is widely preferred due to its implicit features, such as broad noise margin, consumes less power and less reactive when device parameters are modified. NMOS acts as a pull-down device in CMOS technology whereas PMOS or a resistor acts as a pull-up device. When pull-down device (NMOS) is inactive, the output is pulled high due to ON state of pull-up device. When pull-down becomes active, the output is pull-down to GND voltage. In order to maintain the output close to threshold levels, the loads are selected to have weak values. This is helpful in providing accurate binary values both '1' and '0'. CMOS technology produces large amounts of gate delay with large noise but the output remains stable. Other advance technologies can also provide better outcomes when compared to CMOS for one or the other applications.

2.1.2 Ratioed Logic Technique: For few applications Ratioed technology based on W/L ratios of NMOS and PMOS provides great outcomes. However, it has few confinements on the ratio of pull-up and pull-down devices. If pull-down is high, then output will appear after limited delay and large amount of static power is utilized but noise margin gets shrinked.

In order to overcome above confinements, a single PMOS device with the gate terminal grounded is kept ON throughout the operation. The width of the NMOS transistor is selected to be four times greater than that of PMOS transistor. By this, noise margin is improved and propagation delay is decreased.

2.1.3 Pass Transistor Logic: For data transfer switching circuits pass transistor technology is used. In this mode of operation, drain and source terminal of MOSFET is provided with inputs. NMOS transistor or PMOS transistor or parallel combinations of both are used to build switches.

2.1.4 Transmission Gate Technology: In transmission gate technology, NMOS and PMOS are connected in parallel. It has good speed and power features when compared to CMOS technology. Due to parallel connection, PMOS provides accurate logic '1' and NMOS provides accurate logic '0' pass transistors technology which provides stable output can be effectively used to built full-adders.

2.2 Binary Adder Circuits

2.2.1 Ripple carry adder (RCA): Ripple-carry-adder is the highly preferred traditional configuration. It is executed by combining full-adders. Each full-adder performs addition of three inputs. The resulting outputs are sum and a generated carry. Lot of delay is occurred in forwarding carry bit from start to end-bit. This delay maximizes as the number of input-bits increases. To speed-up the addition, other configurations have been implemented.

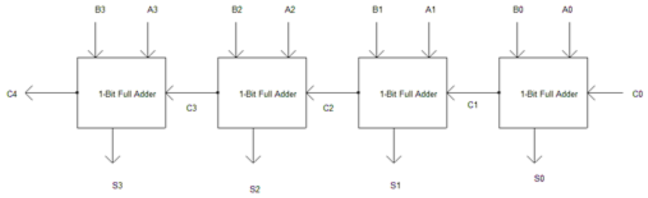


Fig. 1 Ripple Carry Adder (RCA)

2.2.2 Carry-look-ahead adder (CLA): This method considers two input bits A_i and Bi. These two inputs are utilized to execute propagated carry bit (Pi=Ai EXOR Bi) and generated-carry-bit (Gi = Ai AND Bi). Carry bit Ci for second input-bit pair is executed by utilizing Pi and Gi.

This methodology permits to execute sum-bit of each input-bit-pair simultaneously. $C_{i+1}$is executed by a module called CLA generator. Since the fastness of CLA didn't rely on the number of input bits, this method leads to instant addition. Moreover CLA is highly composed than RCA. The complication rises gradually as the number of input-bits rises.

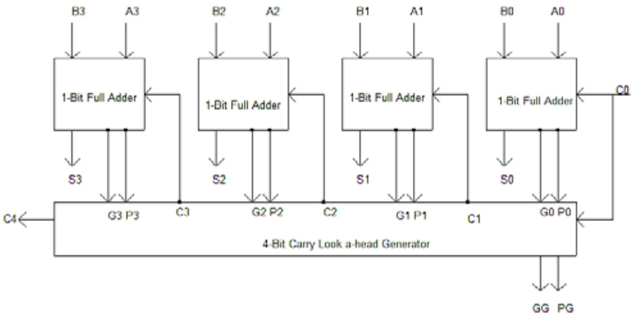


Fig. 2 Carry Look-ahead Adder.

2.2.3 Carry-skip adder (CSKA): This seems to be very high speed configuration among others. This configuration has a skip sub-module. All the propagated values of each input bit-pair are ANDed and assigned as BP. As the name implies, this methodology skip the carry-bit if BP=0. If BP=1, then the carry-bit is rippled. This procedure sounds as if carries are skipped off. This configuration is helpful in decreasing delay to large extent by eliminating group of carries when BP=0. However, it needs minor chip area and occupies a few watts of power when considered to CLA.

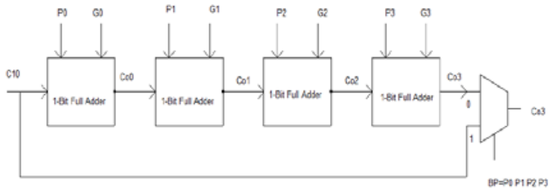


Fig. 3 Carry Skip Adder (CSKA)

2.2.4 Carry-select adder (CSA): This configuration is associated with 2 series of adders. Each set induces two output, sum-bit and output-carry-bit. First series consider input-carry-bit as ‘0’ and second consider it as ‘1’.During execution, when C_{in} is allotted, particular output is picked-up out of two set of series. In order to equate delay of RCA with carry select adder the aspect rations of transistors are varied continuously.

The total number of addition operations performed is [m-1], m is number of input bits. The execution is carried out by adding starting input-bits-pair, then the resulting sum is added to next-bit pair and this continued up to mth bit. This methodology is composed of two sets of RCA and required 2:1 multiplexers in order to select one set of RCA output. Since, it occupies large amount of microchip area, it is not considered for ALU architecture.

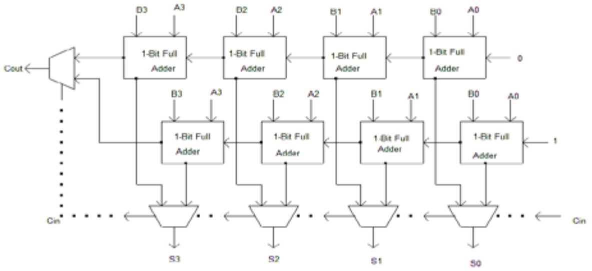


Fig. 4 Carry Select Adder (CSA).

3. THE ALU DESIGN

A 32-bit ALU design is considered to perform 16 different operations such as addition, subtraction, multiplication, division, increment, decrement, shift, NOT, AND, NAND, OR, NOR, XOR, XNOR etcetera. Different logic technologies provide their own advantages. Various technologies are preferred for design of various modules of ALU. Selection of different logic techniques have their own standards for optimum operational performs of ALU.

The full-adder is considered to be very necessary part of ALU, because it identifies the overall operations of ALU. The full-adder module is consisting of several sub-modules. The fundamental sub-module is EX-OR logic gate. Addition operation can be easily performed with the help of EX-OR gate. Input-bits are negated in order to perform subtraction operation. Input-bits can be negated by using NOT gate resulting as one's compliment. Logic '1' is assigned to Cin (input carry) giving two's compliment of the subtrahend and one's compliment of minuend will be added together by full-adder module to give subtracted output. Multiplexers have a feature of utilizing fewer amounts of power and delay. For effective design method of 32-bit ALU, multiplexers are used.

3.1 Single bit ALU design: Arithmetic and logical functions are separately simulated and verified at RTL (resistor transistor level) and gate level. In order to form a single bit ALU initially, individual arithmetic and logic modules are combined. An obtained single-bit ALU can perform 16 different operations. This single bit ALU will be simulated and verified. Simulation results determine propagation delay, occupied area and power of single bit ALU. A 4-bit ALU will be formed by combining four separate single bits ALU. Moreover, 32-bit ALU can be obtained by combining eight separate 4-bit ALUs.

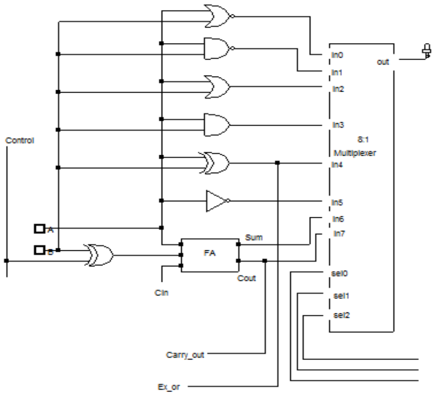


Fig. 5 Single bit ALU.

3.2 4-bit ALU Design: By combining four single bit ALUs executing four different functions give us 4-bit ALU design. The four functions taken into consideration are AND, OR, XOR and addition. Each function is provided with input bits. The inputs A and B are of 4-bit each. The outputs of each function module are given to 4:1 multiplexer. Multiplexer select one among four outputs with the help of select lines S_o and S_1. Only one function will be performed at a given time.

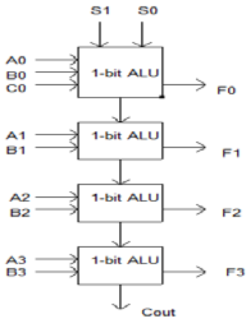


Fig. 6 4-bit ALU Design

3.3 32-bit ALU design: Execution standards are minimum delay, less area and power occupied. 32-bit ALU is composed of many modules. Each module designed separately in order to meet optimum execution standards. The implementations of fundamental logical operations are done using CMOS technology. Implementation of 16:1 multiplexer is done using NMOS technology. The 16:1 multiplexer is utilized to select one out of 16 arithmetic and logic operations. Multiplexer is taken into consideration due to its plenty of features such as, area is minimized and delay is reduced. Since less area is occupied power consumption is also reduced.

Different adder module configurations are studied in detail and it is resulted as carry skip adder meets the entire execution standard in terms of power, area and delay. Carry skip adder is derived from ripple carry adder. Carry bit of each adder in CSKA is ANDed. This ANDed value is provided as input to 2:1 multiplexer. If the AND output is binary '1', then carry-bit will be selected otherwise input carry-bit will be selected. Since, ripple carry path is avoided by carry skip adder configuration. This implementation is selected in many cases. After studying the entire adder configuration in detail, the designer selects carry skip adder configuration as it meets all the execution standards. Complexity to design carry look-ahead adder and carry select adder increases with the number of input bits.

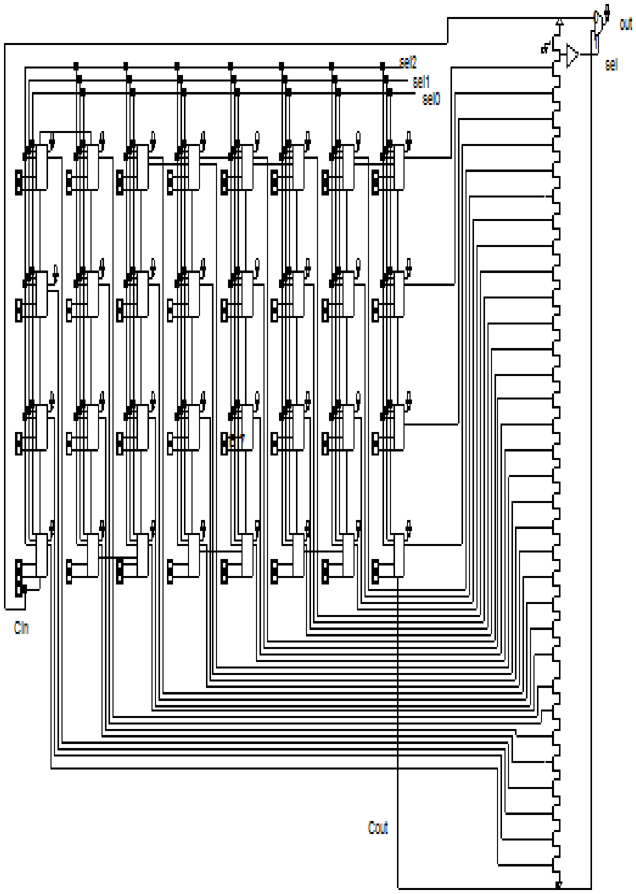


Fig. 7 32-bit ALU Design

Output generated by carry skip adder module is provided to 2:1 multiplexer module. Multiplexer module prefers transmission gate technology for the implementation. Transmission gate have best features incorporated within it, such as it can produce accurate zero and accurate one output values. Moreover, it is influenced by less delay.

4. ALU Operation

ALU is considered to execute two forms of functions. First part describes evaluation of arithmetic functions. Second part describes evaluation of logical functions. The capability of evaluating different arithmetic and logic computations is called specification of ALU. 2:1 Multiplexer is used to select one among two forms of computations. Multiplexer is consisting of two select lines in order to control the execution.

A 16-input pseudo-NMOS AND module is used to execute AND operation in

5. 32-BIT ALU SIMULATION

ALU design is consisting of 32-input-bits. It is simulated in Model Simulator. A and B are the two 32-bit inputs. Mode is a 1-bit signal that is used to select either arithmetic or logic functions. Mode=0: selects logical operations, Mode=1: selects arithmetic operations, SEL is 4-bit signal use to select one among sixteen different logical functions when Mode=0.

For example SEL=0: selects OR function, SEL=1: selects AND function, SEL=2: selects XOR function and SEL=3:selects NOT function. CIN is 1-bit signal which is used to select one among two arithmetic functions. CIN=0: selects addition operation and CIN=1:selects subtraction operation.

OUT is a 32-bit output-sum. Cout is a single-bit output carry. Signal ‘V’ switches to binary ‘1’ when register overflow occurs. Signal ‘N’ switches to binary ‘1’ when the negative value is detected. Both ‘V’ and ‘N’ are of single-bit.

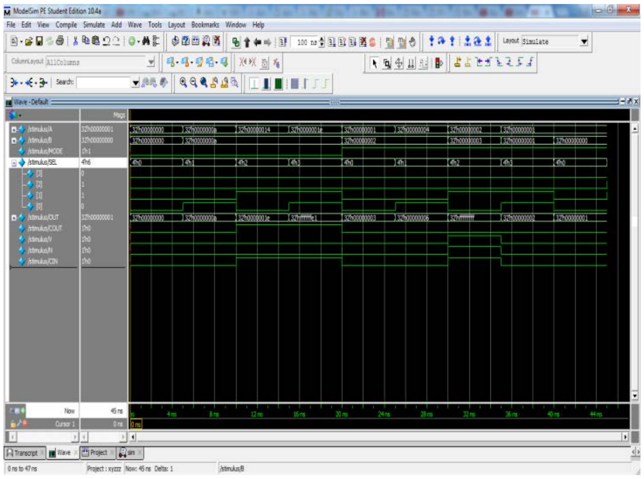


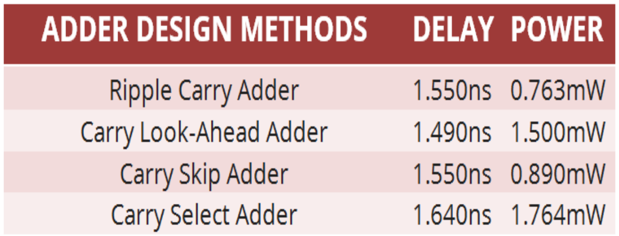
Fig. 8 Simulation Results of 32-Bit ALU

6. COMPARISONS

All the four configurations are simulated and comparison table is given below. From the table, it is clear that Carry-Look-ahead Adder is producing very less delay, but the implementation becomes very difficult as the number of input bits increases. Since area occupied by Ripple-Carry-Adder is small compared to other configurations, it consumes less power.

But it introduces large amount of delay. Carry-Select-Adder introduces large amount of delay, occupy more area and consumes high power. Hence these three configurations are not used to design an ALU. Carry-Skip-Adder seems to be the best method of designing an adder because it meets all the execution standards.

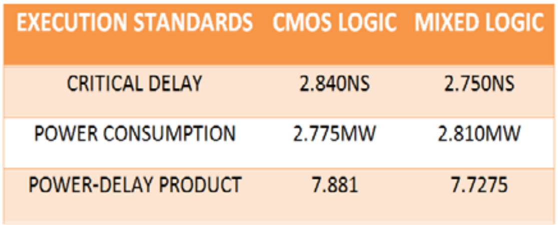
Table 1: Comparison of Adder Configurations



ADDER DESIGN METHODS	DELAY	POWER
Ripple Carry Adder	1.550ns	0.763mW
Carry Look-Ahead Adder	1.490ns	1.500mW
Carry Skip Adder	1.550ns	0.890mW
Carry Select Adder	1.640ns	1.764mW

Carry-Skip-Adder is designed using CMOS and Mixed-Logic. By referring below table, it is clear that Mixed-Logic gives better results than CMOS technology.

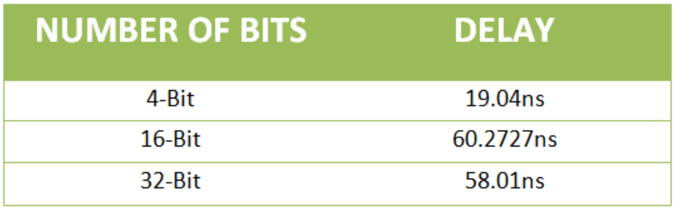
Table 2: Mixed-Logic and CMOS Comparison



EXECUTION STANDARDS	CMOS LOGIC	MIXED LOGIC
CRITICAL DELAY	2.840NS	2.750NS
POWER CONSUMPTION	2.775MW	2.810MW
POWER-DELAY PRODUCT	7.881	7.7275

In the following table delay for different number of bits are compared. It is clear from the table that 16-bit ALU introduce large amount of delay. Since each component of an ALU is analyzed in detail, delay at the component level is reduced. Those components, whose delay has already minimized, can be used to obtain 32-bit ALU with small amount of delay.

Table 3: Comparison of Different bits of ALU in terms of Delay



NUMBER OF BITS	DELAY
4-Bit	19.04ns
16-Bit	60.2727ns
32-Bit	58.01ns

7. CONCLUSION AND FUTURE SCOPE

Four different Binary Adder Configurations are introduced and described in detail. Code is generated in verilog (HDL) language for all the configurations. Simulation of the code is done on Model Simulator. All the configurations are compared with respect to execution specifications. Carry-Skip-Adder configuration meets all the execution standards. Hence it is used to design an ALU of 32-bit. Transistor logic families are studied in detail.

Different technologies are compared in terms of power and delay. Mixed logic is preferred for designing Carry-Skip-Adder Module because it consumes less power and introduce less delay. After completing the design of 32-bit ALU, simulation is performed. This simulated code of a 32-bit ALU design is implemented on FPGA SPARTAN-3E board. Resulting 32-bit ALU is capable of operating 16 different arithmetic and logic functions. Continuous research is on implementing ALU with more and more number of input bits. Designers are studying the internal part of each components of an ALU, in order to overcome delay problem. As the numbers of input bits are increased, occupied area also increases. Now the plan is to implement ALU with more number of bits by maintaining the same area. Designers are aware that fabrication process introduces error because of the usage of large capacitance. Now, the time is to turn towards smaller capacitance. Logic Designs that are realized by smaller capacitance, consumes less power and optimizes area efficiently.

REFERENCES

1. C srinivasan, "arithmetic logic unit design using reconfigurable CMOS logic". Mysore university etd-1011103-211310, December 2003:

2. Neil Weste. David Harris, "CMOS VLSI Design: A circuits and systems perspective", fourth Ed.., Pearson Ed.., ISBN 13:978-0-321-54774-3, 2011

3. Yingtao Jiang, Abdulkarim AL-Sheraidah, Yuke Wang, Edwin ShaJin-Gyun Chung, " a novel multiplexer-based low power full adder", IEEE Transactions on Circuits and systems- II VOL.51, NO.7, July 2004

4. Burgess, N. "Fast Ripple-Carry Adders in Standard-Cell CMOS VLSI" 20th IEEE Symposium on Computer arithmetic. Pp. 103-111, 2011

5. R. Zlatanovici, S. Kao, and B. Nikolic, "Energy-Delay Optimization of 64-bit carry look-ahead adders with a 240ps 90nm CMOS design example", JSSC, vol.44, no. 2, pp. 569-583, February 2009

6. International Journal of Emerging trends and technology in computer science vol. 1, issue 2, ISSN 2278-6856. July-August 2012

7. S Anusha et al. Int. Journal of Engineering research and applications. ISSN: 2248-9622, vol.4 Issue 4 (version 8), April 2014, pp. 86-91