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A 32-Bit RISC Processor for Convolution Application

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Abstract
Digital signal processing applications widely use convolution as an important operation, many algorithms have been proposed in order to improve the potential of the filters used. The contemplated RISC processor follows Von Neumann architecture and the processor is non-pipelined, having load store architecture and 32 bit instruction format. The processor possess arithmetic instructions, logical instructions, instructions which operate on data directly, instructions which pause the processing until the next interrupt is accessed, jump instructions, load and store instructions. The proposed design has high speed, low power and area efficiency.

The contemplated architecture uses 4 bit circular convolution and the time taken to perform 4 bit circular convolution is 270ns and 5ns are needed to execute a single instruction. The proposed processor uses 3195 look up tables and 315 logic elements, which defines its area efficiency

Keywords: RISC Processor, Von Neumann Architecture, Circular Convolution, Digital Signal Processing.

1. Introduction

The processing of tasks is being carried by the three major components in technology they are microcomputer, microprocessor and microcontroller. In microcomputer the processing element is central processing unit and the processing is carried with the help of memory elements and I/O ‘s. Microprocessor is fabricated on the silicon chip and the processing is carried with the help of arithmetic and logic unit, registers, memory and control unit . Microcontroller is the one fabricated on silicon chip and consist of microprocessor and various elements like I/O ‘s, memory, timers, counters etc.

The word microprocessor consists of two words micro and processor. The word micro implies small and processor implies processing the data in the form of 0’s and 1’s. The word micro changed its meaning over a period of time and now the technology is in terms of small chip holding billions of devices.

Microprocessor is a device which can be programmed, it takes input in the form of binary format and performs processing of operations in arithmetic and logic unit and gives the output in the binary format which is then converted to user friendly conversions and the result so generated is stored in memory.

2. Literature Review

The first reference proposed a design methodology of a single clock cycle MIPS RISC processor using VHDL to ease the description, verification, simulation and hardware realization [1]. It follows R format which has 6 bits for opcode and 25 bits being distributed as, 5 bits each belonging to Rs, Rt, Rd, shift and function. I format which has 6 bits for opcode, 5 bits for Rs, 5 bits for Rt and remaining 15 bits for address or immediate value. J format has 6 bits for opcode and 25 bits for branch target address.

The second reference proposed processor which has Harvard architecture and consists of 24 bit address, 5 stage pipeline instruction execution and internal debug logic [2]. It has 2 block repeater and for execution of operations it has 16 bit ALU, 16 bit multiplier and 16 bit barrel shifter. It has 2 interfaces one is internal interface and other is external interface, the former uses JTAG protocol and the later uses scan chain. Interface to AMBA system is carried with the help of AMBA AHB master wrapper.

The third reference proposed processor which works on the design and verification of a 32 bit general purpose microprocessor which is compatible with ARM7 RISC core [3]. The design of the processor is divided into three stages implying pipeline stage analysis, RT level functional unit composition and control signal generation. The processor is being designed to successfully implement ADPCM, SOLA and MP3 algorithms.

The fourth reference has described the architecture and design of the pipelined execution unit of a 32 bit RISC processor. Core –I is a processor which is 32 bit based on RISC architecture [4]. The execution unit has six stages of pipeline and is based on the load store architecture. Both single precision and double precision floating point operations are carried.

The fifth reference has proposed the architecture and have implemented programmable video signal processor dedicated as building block of a multiple instruction multiple data (MIMD) based bus connected multiprocessor system is presented [5]. The video standards followed in the above design are H.261, H.263, MPEG-1 and MPEG-2.

The sixth reference has proposed a parallel MAC (multiply accumulation) architecture designed for DSP applications on a 200 MHz, 1.6 GOPS multimedia RISC processor [6] . The floating point coprocessor which is 64 bit has a datapath which realizes parallel operations which are done on short words like parallel four SIMD 16 bit arithmetic operations

The seventh reference discusses a VLSI based multiprocessor architecture for real time processing of video coding applications [7] . The processor uses hybrid coding algorithms where in the coding scheme consists of motion estimation, discrete cosine transform, run length coding, inverse quantization, reconstruction, filtering and predication, quantization, variable length coding and inverse discrete cosine transform.

The eighth reference has been presented 16 bit non pipelined RISC processor for its application towards convolution. The ALU design of the processor uses modified Wallace tree multiplier which has high speed and low power. The program counter in the processor is the design of an incremented structure and is implemented using quasi adiabatic 2N-2N2P logic structure.

3. Design of RISC CPU (32-Bit)

3.1 Architecture

The processor is designed initially with 27 instructions and each instruction has a uniform 16 bit format. The instructions here are single cycled and non pipelined. The processor design uses a common memory bus for both instructions and data that is it follows Von Neumann architecture. The processor possess arithmetic instructions, logical instructions, instructions which operate on data directly, instructions which pause the processing until the next interrupt is accessed, jump instructions, load and store instructions. The proposed design as shown in figure 2 has high speed, low power and area efficiency. The design details of each block are as follows.

3.1.1 Program Counter:

The 32 bit RISC processor possesses a program counter which is 32 bit where in 6 bits are used to indicate the location in instruction memory. As architecture followed in the design is load store architecture in order to execute a load store instruction the program counter uses additional 6 bits to point to data memory.

3.1.2 Arithmetic and Logic unit

The arithmetic and logic unit performs arithmetic operations like addition and subtraction with the help of sign flag and zero flag. There are also shift and rotate operations carried out with specific numbers of bit.

3.1.3 Register file

As the processor is of 32 bit capacity the registers are also of 32 bits. There are eight general purpose registers. Arithmetic and data centric instructions are carried out with help of registers. There are load and store instructions, the load instruction is used to place the values in the registers and the store instruction is used to get the processed values from the processor to the memory

3.1.4 Instruction Fetch Unit

The function of this unit is to take the address of the program counter and fetch the instruction from the memory at that particular address. The next instruction is obtained by increasing the current value of the address held at the program counter by four. There are two types of addressing used here one is byte addressing and the other is word addressing. Figure 1 shows the block diagram of instruction fetch unit.

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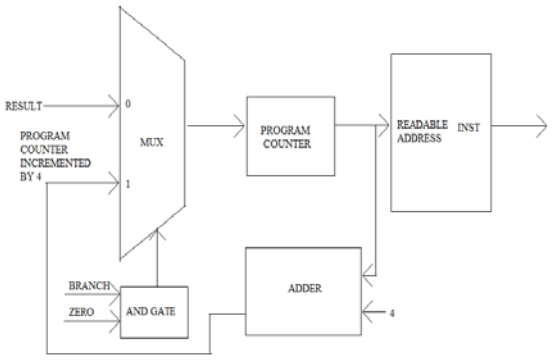

Fig. 1: Block diagram of instruction fetch unit

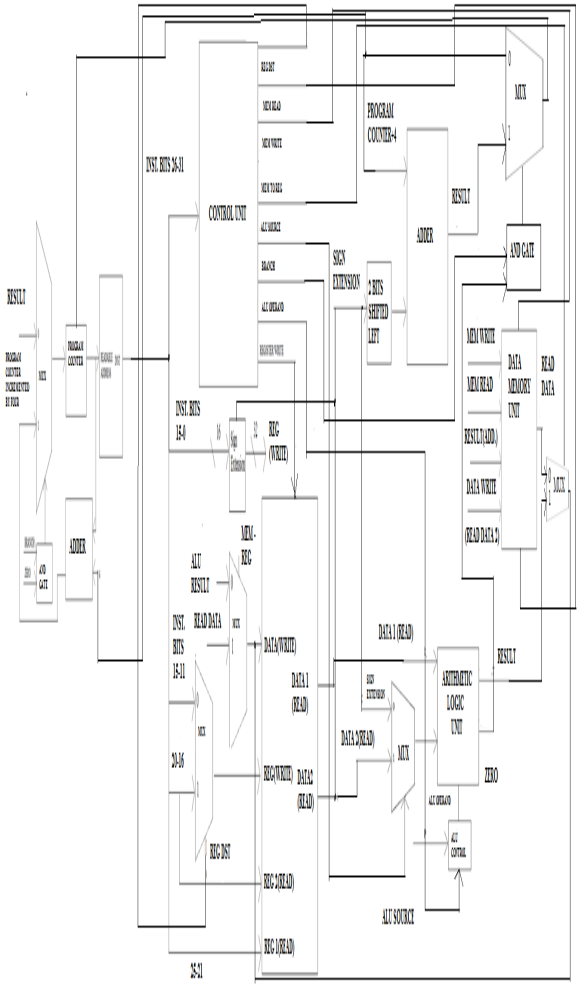

Fig.2: Proposed architecture

3.1.5 Instruction Decode Unit

The instruction fetch unit provides the instruction to the decode unit , this unit will indicate the registers and access the data values present in the register as shown in the figure 3.

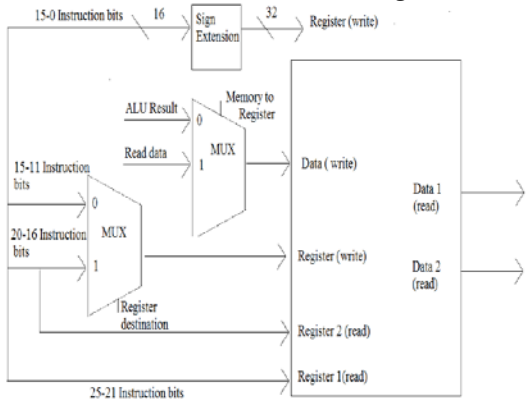

Fig. 3: Block diagram of instruction decode unit

3.1.6 Control Unit

The instruction opcode from 26-31 bits in the instruction indicates the control signal. There are nine control signals as shown in the figure 4.

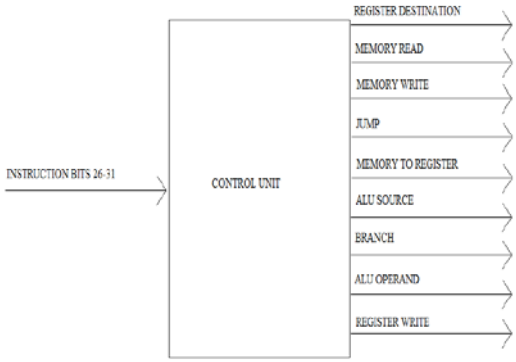

Fig. 4: Block diagram of control unit

3.1.7 Execution Unit

The operation to be performed is determined by the ALU operand present in the instruction, the operation is executed by the arithmetic and logic unit. In order to obtain the branch address value, the sign extended value is obtained then it is shifted by 2 bits to the left, the obtained value is then added to PC + 4, this is carried by the separate unit present in the execution unit that is adder. Figure 5 shows the block diagram of execution unit.

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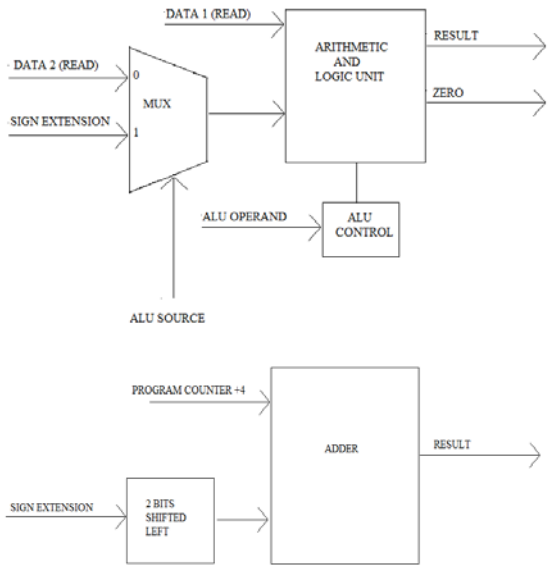

Fig.5: Block diagram of execution unit

3.1.8 Data Memory Unit

The data memory unit is used when the load and store instructions are executed. The data memory unit has ALU result, Read data 2, Memwrite, Memread as inputs and the Read data and Data memory are the output's.. Figure 6 shows the block diagram of data memory unit.

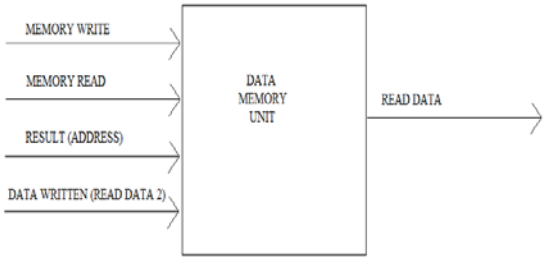

Fig.6: Block diagram of data memory unit

4.Circular Convolution

Convolution is defined as a mathematical operation performed on two functions one is the input x[n] and the other is the finite impulse response h[n] to produce y[n] the output.. The procedure to perform 4 bit circular convolution is as follows:

1) Draw a circle and label it with input x[n] in clockwise direction outside the circle as shown in the figure 7 with x[n]={1, 1, 0, 2} and h[n]={2, 5, 4, 3}

2) The inner part of the circle is labeled in with h[n] in anticlockwise direction.

3) Multiply the terms and add to produce y[0] as seen in the figure 7.

4) Keeping the terms of the input x[n] fixed, rotate the terms of h[n] in anticlockwise direction by one term and repeat step 3 to get y[1] .

5) Repeat the above procedure to obtain y[2] and y[3].

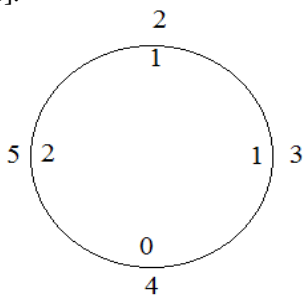

Fig.7: Computation of y[0]
Y[0] = 2+3+0+10 = 15

5. Simulation Results

5.1 Instruction fetch unit

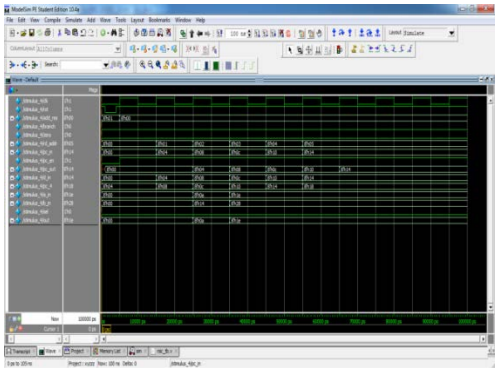

Fig.8 : Simulation result of instruction fetch unit.

5.2 Instruction decode unit

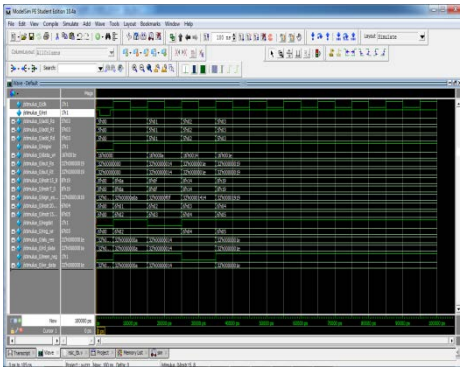

Fig.9: Simulation result of instruction decode unit

5.3 Control Unit

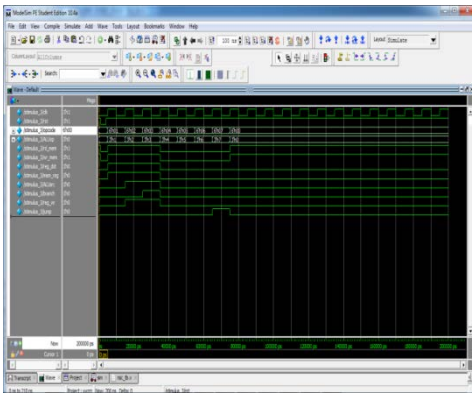

Fig.10: Simulation result of control unit

5.4 Execution Unit

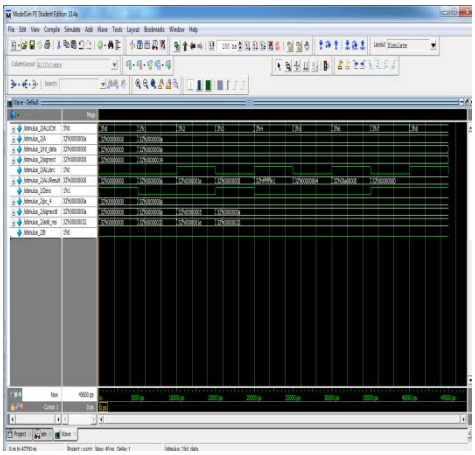

Fig.11: Simulation result of execution unit

5.5 Simulation result of RISC processor

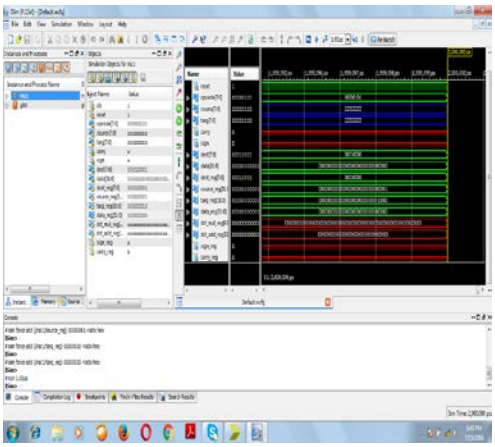

Fig.12: Simulation result of RISC processor with circular convolution.

6. Future Scope and Conclusion

The implemented 32 bit RISC processor can be used to perform image convolution, 2D linear convolution and circular convolution for large number of bits which can be used in digital signal processing applications.

7. Comparison Table

Table 1:Comparitive Study

Parameters	Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]	Proposed Work
Implementation	FPGA	FPGA	FPGA	FPGA	FPGA
Frequency	200 MHz	50 MHz	50 MHz	16 MHz	270 MHz
Area	-	-	78 CLBs and 6 DSP elements	65012 nm^2	2980 LUTs

References

[1] Reaz, M.B.I. , Islam, M.S.; Sulaiman M.S.;"A single clock cycle MIPS RISC processor design using VHDL", Semiconductor Electronics, 2002. Proceedings ICSE 2002. IEEE International Conference. ISBN: 0-7803-7578-5; Issue Date: 19-21 Dec. 2002

[2] Seung Pyo Jung; Jingzhe Xu; Donghoon Lee; Ju Sung Park; Kang-joo Kim; Koon-shik Cho; "Design & verification of 16 bit RISC processor". SoC Design Conference, 2008. ISOCC'08. International; ISBN: 978-1-4244-2598-3; Issue Date:24-25 Nov. 2008

[3] Geun-young Jeong; Ju- sung Park; Hyun-woo Jo; Byung-woo Yoon; Myung-jinLee; "ARM7 compatible 32-bit RISC processor design and verification", Science and Technology, 2005. KORUS 2005. Proceedings. The 9th Russian-Korean International Symposium on; July 2005.

[4] Shofiqul Islam; Debanjan Chattopadhyay; Manoja Kumar Das; V Neelima; Rahul Sarkar; "Design of High-Speed-Pipelined Execution Unit of 32-bit RISC Processor"; India Conference, 2006 Annual IEEE.

[5] Hermann, K..; Otterstedt J.; Jeschke, H.; Kuboschek, M. "A MIMD-based video signal processing architecture suitable for large area integration and a 16.6-cm/sup 2/ monolithic implementation", Very Large Scale Integration(VLSI)Systems, IEEE Transactions on, Volume: 6, Issue: 2.

[6] Kuroda, I.; Murata,E.; Nadehara, k.; Suzuki, K.; Arai, T.;Okamura, A.; "A 16- bit parallel MAC architecture for a multimedia RISC processor", Signal Processing Systems, 1998.SIPS 98. 1998 IEEE Workshop ON, ISBN: 0-7803-4997-0, Date: 8-10 Oct 1998.

[7] Jeschke, H.; "A VLSI based multiprocessor architecture for video signal processing", Circuits and Systems, 1992.ISCAS'92. Proceedings. 1992 IEEE International Symposium on, ISBN: 0-7803-0593-0, Date: 3-6 May 1992.

[8] Samiappa Sakthikumaran, et al, "16-Bit RISC Processor Design for Convolution Application", in IEEE-International Conference on Recent Trends in Information Technology, (ICRTIT 2011), MIT, Anna University, Chennai. June 3-5, 2011.

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