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Study of Power Distribution Techniques for VLSI Design

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ABSTRACT

In the past two decades, CMOS-VLSI Technology has rapidly embraced the field of analog integrated circuits, providing low-cost, high performance solutions and to dominate the market. Lowering the supply voltage is the most effective way to achieve low power performance became power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage low power has emerged as a main theme in electronic industries today on the other hand energy efficiency is one of the most critical feature of modern electronic world. Electronics industry wants to designed high speed, high performance and compact devices according to consumer demands. Reduction the power consumption makes a device more reliable and efficient. The portability requirement of hard-held devices and other portable instruments places severe restrictions on size and power consumption. Even through battery technology is improving continuously and processors displays are rapidly improving in terms of power consumption, battery life, weight are the major issues influence low the hand-held instrument can be used. This paper presents the review the various consumption & management techniques for low power and systems

Keywords: VLSI, consumption, low power, CMOS, high performance, battery.

Introduction

Portable systems are being used increasingly because these systems are battery increasingly because these systems are battery powered reducing energy consumption is vital (i). In this paper we give an overview of low power design and provide a review of techniques to exploit them in the architecture of the system. Low power consumption is very important and challenging factor amongst the engineers, scientists & researchers. Power consumption is one of the top issue in VLSI-CMOS circuit design for which, CMOS is the prominent technology Today's focus on low power is not only because of recent growing demands of devices have created a growing demand for energy efficient circuit design. However there is no universal cut tradeoff between power consumption, delay and area [2]. Therefore designers are required to select suitable and efficient techniques that satisfy the application and product need [3]. The aim of this paper is to show how devices, circuits and architectures within this design space may be optimized for minimum energy consumption. The new strategies are necessary to address the power concerns in high performance designs.

There are several VLSI techniques to reduce leakage power, input rise time, source leakage current, gate current. Switching power,short circuit power, power in capacitance, and also dissipation in output loading effect the power consumption of device [4]. Currently sub-threshold leakage seems to be the main contribution factor as compare to all type of leakage power [5]. In this paper we propose a new approach, thus providing a new choice to implement low-power VLSI circuit design. The proposed power consumption techniques in CMOS logic family and describe the methods for evaluation both static and dynamic power dissipation.

Low Power Design

Total power dissipation is the sum of the static and dynamic dissipation components. Dynamic dissipation has historically been for greater than statics power when systems are active and hence, static power is often ignored, although this will change as gate and sub threshold leakage increase. Power dissipation has become extremely important to VLSI designers. For high performance systems such as workstations and servers, dynamic power consumption per chip is often limited to about 150 w by the amount of heat that can be managed with air-cooled systems and cost-effective heat sinks. This number increases slowly with advances in heat sink technology and can be increased significantly with expensive liquid cooling but has not kept pace with growing power demands of systems. Therefore performance may be limited by the inability to cool huge systems with power hungry circuits operating at high speed. For battery systems such as Laptops, cell phones, and PDAs, power consumption sets the battery life of the product.

Dynamic Power Reduction Techniques

It the process is selected with sufficiently high threshold voltage and oxide thickness, static dissipation is small and dynamic dissipation usually dominates while the chip is active show that dynamic power is reduced by decreasing the activity factors the switching capacitance, the power supply or the operating frequency.

The dynamic power dissipation is given as :

$$\mathbf{P_{dynamic} = \alpha\, C V_{DD}^2 f}$$

Where α – activity factor

f – clock frequency

V_{DD} – supply voltage

A clock has an activity factor X=1 because it rises and falls every cycle. Most data has a maximum activity factor of 0.5 because it transition only once each cycle static CMOS logic has been empirically determined to have activity factors closer than 0.1 because some gates maintain one output state more often than another and because real data inputs to some positions of a systems often remain constant from once cycle to the next. Interconnect switching capacitance is most effectively reduced through careful floor planning, placing communicating units near each other

to reduce wire lengths. Voltage has a quadratic effect on dynamic power. Therefore, choosing a lower power consumption. As many transistors are operating in a velocity started region, the lower power supply may not reduce performance as much as first order models predict.

Commonly used metrics in low power design are power delay product and energy delay product. Power alone is a questionable metric because it can be reduced simply by computing more slowly. The power delay product also suspect because the energy can be reduced by computing more slowly at a lower supply voltage.

Static Power Reduction Technique

Static power reduction involves minimizing static some circuit techniques such as analog current source and pseudo n MOS gates intentionally draw static power they can be turned off when they are not needed.

Sub threshold leakage current for Vgs < Vt is

$$Ids = I_{dso}\, e^{Vgs-Vt/nVt}\ [1\text{-}e^{Vds/Vt}]$$

Where the term n describes drain-induced barrier lowering Sub threshold leakage power is already a major problem for battery powered designs in the 180 nm generation and will be growing exponentially as power supplies and threshold voltages are scaled down in future processes many low power systems need high performance while active and low leakage while idle. The high performance requirement entails relatively low thresholds which contributed excessive leakage current in the idle mode In low power battery operated devices, leakage specifications may be given at 400 C rather than 1100 C because battery life is most important in the range of normal [6] ambient temperature [8].

CMOS Model

Most components are currently fabricated using CMOS technology. Main reasons for this bias is that CMOS technology is cost efficient and inherently lower power than other technologies. The sources of energy Consumption on a CMOS Chip can be classified as static and dynamic power dissipation. The main difference between them is that dynamic power is frequency dependent, while static is not. Bias (P_b) and leakage currents (P_l) cause static energy consumption. Short circuit currents (P_{sc}) and dynamic energy consumption (P_d) is caused by the actual effort of the circuit to switch

$$P = P_d + P_{sc} + P_b + P_l$$

Actually the contributions of this static consumption are mostly determined at the circuit level [9]. Dynamic power can be partitioned into power consumed internally by the cell and power consumed due to driving the load.

Load Power is used in charging the external loads driven by the cell, including both wiring and fan-out capacitances. So the dynamic power for an entire chip is the sum of the power consumed in driving all the load capacitances.

A first order approximation of the dynamic energy consumption of CMOS circuitly is given by the formula

$P_d = C_{eff} V^2 f$

Where P_d is the power in watts, C_{eff} is the effective capacitance in Farads, V is the supply voltage in volts and f is frequency of operations in Hz [10].

Ceff combines two factors C, the capacitance [7] being charged / discharged, and the activity weighting α which is the probability that a transition occurs.

$C_{eff} = \alpha C$

A designer at the technological and architectures level can try to minimize the variables in there equations to minimize the overall energy consumption [11]

Power modeling and analysis

The search for the optional solution must include at each level of abstraction, a design improvement loop. In such loop a power analysis is estimator ranks the various design synthesis and optimization options, and thus helps in selecting the one that is potentially more effective from the energy consumption stand point.

Power analysis tools are available primarily at the gate and circuit levels and not at the architecture and algorithm levels where could really move an impact, current research is trying to fill this gap [10,13, 14].

Reduce Voltage and frequency

In the present scenario the most effective way is energy reduction of a circuit at the technological level is to reduce the supply voltage, because the energy consumption drops quadratically with the supply voltage for example, reducing a supply voltage from 5.0 volts to 3.3volts reduces power consumption vendors now have low voltage versions. Then the problem arises is that lower supply voltage will cause a reduction in performance [15].

The variable voltage and frequency have a trade off in delay and energy consumption reducing clock frequency f alone does not reduce energy, since to do the some work the system must run longer. As the Voltage is reduced, the delay increases. A common approach to power reduction is to first increase the performance of the module. To enhance the performance by adding parallel hardware and then reduce the voltage as much as possible so that required performance is still reached.

Result and Discussion

As there will become an increasing numbers of portable, battery powered systems, move and more attention will be focused on low power analog circuit design techniques. The art of low power design used to be a narrow specialty in analog circuit design. As the issue of energy efficiency becomes ever more pervasive, the battle to use the bare minimum of energy will be fought on multiple fronts live semi conductor technologies, circuit design, automation tools system architecture, operating system

and application design. At the system level the system designer can take advantage of power management features where available as well as decomposed system architectures and programming techniques for reducing power consumption

Some low power design techniques are also used to design high speed circuits, and to increase performance. For example therefore also consumes less energy. Using a cache in a system not only improves performance but although requiting more space uses less energy since date is kept locally. Energy efficient a synchronous system also have the potential of a performance increase, because the speed is no longer dictated by a flow but is as fast as the flow of data.

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