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Ternary Logic Gates & Arithmetic Circuit

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Abstract

Scaling of conventional CMOS devices has reduced the device dimensions from 10 mm in 1970s to 0.1 μm in a present day.
According to ITRS (i.e. International Technology Roadmap for Semiconductors) we are going to face the brick wall in 2015 if we continue in the same development speed. This will not be possible for us to maintain the pace forecaste byMoore.(Moore's law) This is because of the fundamental limitations of device parameter dimensions due to which performance is degrading in several ways. To overcome this and go ahead in technology , one must look into new devices those can be scaled down to come up with other solutions. Either it should be possible to go ahead by again reducing the device dimensions in some way or we have to reduce the circuit overhead with less complexity. Solution to this might be : MVL i.e. Multivalued Logic & TFET i.e. Tunnel Field Effect Transistor. This report presents a novel design of Ternary Logic Gates & arithmetic circuits using TFET. By using this ternary technology designing of arithmetic circuits can implement.

Keywords*: logic ,ternary ,arithmetic circuits, multivalued logic and TEFT*

1. Introduction

A ternary, three-valued or trivalent logic (sometimes abbreviated 3VL) is any of several multi-valued logic systems.The ternary that is "three valued" has more advantages over binary logic in the design of digital systems. The main advantage of ternary is since each wire can transmit more multi-valued logic information than binary also reducing chip size area. Because of the less estimation interconnection cost it receives more attentation than others . The arithmetic operations and logical operation at higher speed can be done using ternary. Implementation of digital system with these advantages achieved using VLSI and it has very simple electronic design implementation technique. These proposed ternary gates have been useful for the design of "digital system" , such as the implementation of the combinational design like multiplexer, half adder.
(3N – 1)/2
T-gates are required for the implementation of combinational logic circuit, as was demonstrated in but it has some disadvantage which is ,as number of gates more, the design of digital system become more complex. To overcome this disadvantage we have proposed the new ternary design based on MOS technology like INVERTER, AND gates which can be helpful for the design of digital system like multiplexer.The proposed circuits are shown to have some significant advantages relative to other ternary circuits based on the Tgate
like low power dissipation, reduced propagation delay, and also reduced component count. Because of these several advantages these ternary logic have been used in several important field like communication, digital signal processing.As is demonstrated in , this is an application where a significant advantage can be gained by using ternary digital hardware, namely, an increased maximum sequence length can be achieved without increasing the complexity of the digital hardware.The present CMOS technology does not use depletion mode transistors. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time and eliminate depletion mode transistors. The reduction
in the number of transistors is main focus as that enabled a more compact design which utilized the less chip area.

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2.CMOS technology

The current technology trend is CMOS technology which is referred as Complementary Symmetry Metal Oxide Semiconductor or COSMOS. From the words "complementary symmetry" , it is clear that , CMOS uses complementary as well as symmetrical pairs of p-type & n-type MOSFETS for logical function implementation. CMOS technology implements all the digital circuits with the main principle that , they use both p-type & n-type MOSFETs to create a path from input to output through voltage source (Vdd) or ground (Vss). MOOR's law states that , number of transistors per particular chip are going to get doubled at every two years approximately. As stated by MOORE , we are scaling the CMOS devices for further optimization & energy conservation . But now CMOS technology has reached its optimum limit & thus going to face the brick wall in around 2015 if we continue the same way . this is because , scaling down is limited due to certain constraints like power dissipation , degradation in switching performance etc. The main reasons are as stated below :

1. Difficulty in OFF current suppression .
2. Difficulty in increase in ON current .
3. Difficulty in decreasing the gate capacitance.
4. Increase in production & development cost.

3.Ternary logic gates

Ternary Logic is the subset of MVL & a most promising alternative to binary logic design. Using Ternary Logic, it is possible to accomplish simplicity & energy efficiency in modern digital design.Traditionally, digital computation is performed on two valued logic ; that is there are only two values possible : True & False. Ternary Logic has attracted considerable interests due to it's potential advantage over the binary.

For example –

1) It is possible to achieve simplicity & energy efficiency since the logic reduces complexity & chip area.

2) Serial & parallel arithmetic operations can be carried fast if Ternary Logic is employed.

Ternary Logic functions are defined as functions having significance if third value is introduced to binary logic i.e. 0 , 1 , 2 which represent True , Undefined , False respectively. Basic gates & arithmetic circuits can be designed using TFETs.

The basic operations of ternary logic can be defined as follows.

$Xi,Xj = \{0, 1, 2\}$

$Xi + Xj = max\{Xi,Xj\}$

$Xi - Xj = min\{Xi,Xj\}$

$Xi = 2 - Xi$

Here " –" denotes the arithmetic subtraction , the operations "+" & "·" are referred to as the OR ,AND & NOT in ternary logic resp. The fundamental gates in the design of digital systems are the inverter , NOR gate & NAND gate.

The most fundamental building blocks in the design of digital systems are the inverter, NOR gate, and NAND gate. In this section, ternary implementations are proposed for the inverter, NOR gate and NAND gate, in which the static power dissipation is low. Three types of basic ternary operations are defined by

$$XC = \begin{cases} C & if \quad X = 1 \\ 2-X & if \quad X=1 \end{cases} \qquad (1)$$

C in Eq. (1) takes the values of logic 1 for a PTI, logic 0 for a STI and logic -1 for a NTI which correspond to higher level (5), middle level (0) and lower level (-5) respectively.With help of this logic we can design ternary gates and ternary arithmetic circuits.

4.Conclusion

The ternary logic is a promising alternative to the conventional binary logic design technique. The ternary and binary logic gates can be used to take advantage of their respective merits, to improve performance in terms of computation speed and power consumption. Expanding the existing logic levels to higher levels higher processing rates could be achieved. This ternary system is capable of transmitting more information as compare to binary system. The proposed ternary design offers most important advantage that is it has very low power dissipation relative to conventional circuits and that lead to significant reductions in propagation delay. The procedure for designing C MOS ternary combinational circuits can be used to construct CMOS ternary sequential circuits. Ternary logic offers several advantages in the particular area like communication ,memory and digital signal processing. STI, PTI and NTI have been designed for operation at ±5V power supply voltage The Tgate uses a Jk arithmetic circuit and three ternary switches. The Jk arithmetic circuit mainly consists of PTI and NTI apart from NOR, inverter and buffer circuits. Half Adder and

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Full Adder consist of T-gate and Jk arithmetic circuit. The PTI and NTI have been designed using an inverter and pass-transistors at its output. The design of PTI and NTI is fully compatible with current CMOS technology.

5.References

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