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Design of Digitally Controlled Switched Mode Power Supply for Low Power High Frequency Application

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Abstract

This paper describes the design simulation and implementation of digital PID controller for the synchronous buck converter working in Continuous Conduction Mode (CCM) based on Field Programmable Gate Array (FPGA) device. The PID controller is implemented in Xilinx ISE digital design environment with Matlab/Simulink simulation and testing environment, through Xilinx System Generator toolbox. The converter operates at a switching frequency of 500 KHz. First the PID controller is designed using Simulink toolbox from Matlab to generate the required set of coefficients to meet the start-up and the transient characteristics. The controller is then realized using Xilinx System Generator (XSG) block set.

Keywords: *Continuous Conduction Mode; FPGA; XSG.*

1. Introduction

DC-DC switching power supplies are used extensively in all areas of work and daily life. Compared with linear power supplies, Switching Mode Power Supplies (SMPS) provide high efficiency, easy integration, small dimensions and weight. Due to these advantages, SMPS have been widely used in numerous portable personal communication systems such as cell telephones, MP3 player and other PDA products, which have grown explosively in recent years. Being widely used in the new generation portable systems, the regulation requirement for low-power high-frequency integrated DC-DC switching mode power supply converter systems becomes more and more demanding in the industry.

Normally analog control provides a very fine resolution in the output voltage. The output voltage can be adjusted to any arbitrary value, which is only limited by loop gain and noise levels.

Digital control is not new in the field of Power Electronics. Based on Digital Signal Processor (DSP) or other processor, it has been applied for several years in motion control, and in medium to high power line-frequency based application such as rectifier, inverters and uninterruptable power supply (UPS). The advantages of digital controller are,

- Advanced control algorithms implementation
- Flexibility and programmability
- Size miniaturization and high frequency
- Less susceptible to component and variations
- Alleviation for the limitation of bandwidth and large gain variation in control law.

In order to avoid the tedious way of implementing the controller, a newly created simulation toolbox called Xilinx System Generator (XSG) - a toolbox working in the MATLAB/Simulink environment can be used not only to simulate exactly the hardware but also to automatically generate the VHDL code needed for the implementation. The user is provided with a library of blocks representing functions which can be implemented in an FPGA. The use of the XSG has two main advantages over traditional methods. First, the implemented algorithm is guaranteed to function exactly as in the simulation and second, there is no need to create two different models (one for the simulation and one for the implementation).

The paper is organized as follows: Section 2 is small signal mathematical model of buck converter. Section 3 describes detailed design of PID controller and stability of converter. Design flow using XSG is given in Section 4. The simulation results obtained by this control technique are given and compared in Section 5. Conclusions are drawn is section 6

2. Mathematical Model of Buck Converter

The schematic diagram of the proposed dc-dc buck converter system is shown in Fig. 1. The mathematical

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model takes the series resistances of the inductor and the capacitor in to account. The capacitor ESR, R_C, introduces a zero frequency to the transfer function.

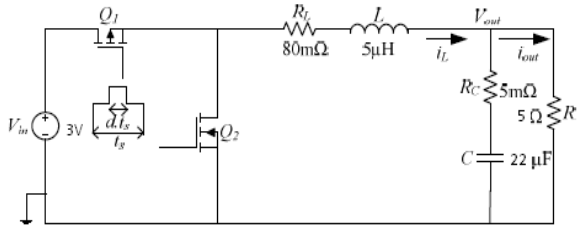

Fig. 1 Buck converter circuit model

Based on the useful state-space averaging model, the transfer functions of a switched buck converter can be developed using small signal analysis. Considering the Current Continuous Condition (CCM) mode, the transfer function of the buck converter can be written in continuous-time *s*-domain

The transfer function for the above buck converter model is found using state space averaging model and is given by:

$$\frac{\widehat{V_{out}}(s)}{\hat{d}(s)} = \frac{(sR_CC+1)V_{in}}{s^2\left(1+{}^{R_C}/_{R}\right)LC+s\left(R_LC+R_CC+{}^{R_LR_CC}/_{R}+{}^{L}/_{R}\right)+{}^{R_L}/_{R}+1} \quad (1)$$

3. Controller Design

Figure 2 shows the overall system model, which contains, the PID controller, the Converter, the ADC and DPWM built from standard Simulink blocks.

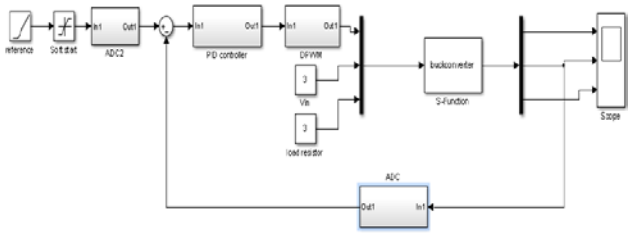

Fig. 2 Block diagram of the complete closed loop system

The PID controller is the most common type of digital control used in digitally-controlled high-frequency and low-power integrated SMPS. Here a discrete-time PID controller is designed to be implemented in FPGA.

3.1 Modeling of PID Controller

Let *e*(*t*) be the input and *d*(*t*) be the output of the controller. A continuous-time PID controller is given by:

$$d(t) = K_P e(t) + K_I \int_0^t e(t)dt + K_D \frac{de(t)}{dt} \quad (2)$$

The discrete-time filtered PID controller can be written as

$$K_{PID}(z) = \frac{r_0 z^2 + r_1 z + r_2}{(z-1)(z+s_1)} \quad (3)$$

Where r_0, r_1, r_2 and s_1 are the controller parameters to be determined by the pole placement method.

The digital control system including the PID controller and a buck converter is shown in figure 3

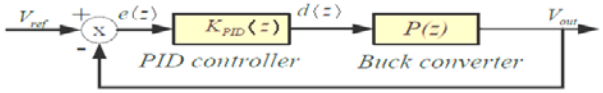

Fig. 3 Block diagram of PID-controlled buck converter

The closed loop transfer function is:

$$T = \frac{V_{out}(z)}{V_{ref}(z)} = \frac{K_{PID}(z).P(z)}{1+K_{PID}(z).P(z)} \quad (4)$$

Setting ${}^{r_1}/_{r_0} = a_1$ and ${}^{r_2}/_{r_0} = a_2$ to cancel the poles of P(z) with the zeros of $K_{PID}(z)$

Then we get

$$\mathrm{T} = \frac{r_0 b_1 z + r_0 b_2}{z^2 + p_1 z + p_2} \quad (5)$$

Where p_1 and p_2 are to be determined by the desired closed-loop dynamics which correspond to the second-order dynamics with a pulsation ω_{cr} and a damping ratio ζ_{cr} (in s-domain $\frac{\omega_{cr}}{s^2+2\zeta_{cr}\omega_{cr}+\omega_{cr}{}^2}$).
Finally the parameters are determined as

$$\begin{cases} r_0 = \dfrac{(1+p_1+p_2)}{(b_1+b_2)} \\ r_1 = a_1 r_0 \\ r_2 = a_2 r_0 \\ s_1 = r_0 b_2 - p_2 \end{cases} \quad (6)$$

The open-loop pulsation can be calculated $\omega_0 = 95346 rd/s$. considering the trade-off between the dynamic behavior and robustness (modulus and delay margins), ω_{cr} is set to 16 times the open-loop pulsation ω_0 corresponding to 1525540rd/s. It can be noted that this pulsation is 15 times smaller than the Nyquist-Shannon sampling frequency (4MHz). With the closed-loop damping ratio $\zeta_{cr} = 0.7$

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$$r_0 = 10.8525, r_1 = -20.7541, r_2 = 10.3011, s_1 = 0.4925$$

Substituting all these values in equation (3) we get the digital PID controller

$$d(k) = r_0 e(k) + r_1 e(k_1) + r_2 e(k_2) - (s_1 - 1)d(k_1) + s_1 d(k_2)$$
$$= 10.8525e(k) - 20.7541e(k_1) + 10.3011e(k_2) + 0.5075d(k_1) - 0.4925d(k_2)$$

The buck converter stability for both open loop and closed loop is found using bode plot which is shown in figure 4. The phase margin is positive value in both the cases.

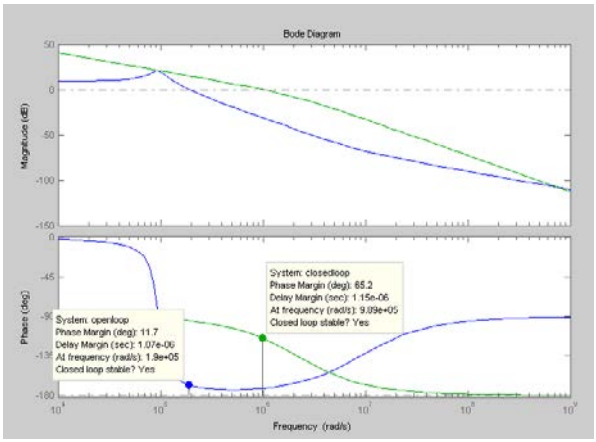

Fig 4 Bode Plot of the Closed Loop and Open Loop Converter.

4. Design Flow Using System Generator

Xilinx System Generator (XSG) for DSP enables control engineers to design and implement their systems in the familiar Simulink environment and then implement it on an FPGA, without the knowledge of a Hardware Description Language (HDL). Such solution shortened the design and testing time, allowing for integration of simulated FPGA project with MATLAB model of the converter. The integrated software design platform containing MATLAB R2010a with Simulink from Math Works, System Generator 13.2 for DSP and ISE 13.2 from Xilinx present such capabilities. Xilinx ISE 13.2 foundation software is not directly utilized and is running in the background when the System Generator blocks are implemented. The XSG environment allows for the Xilinx line of FPGAs to be interfaced directly with Simulink.

The System Generator based discrete PID controller developed for the buck converter is shown in Fig. 5. The controller is designed using the basic building blocks from XSG library as no transfer function block is available. This is just the equivalent implementation of the controller for already designed controller by Simulink.

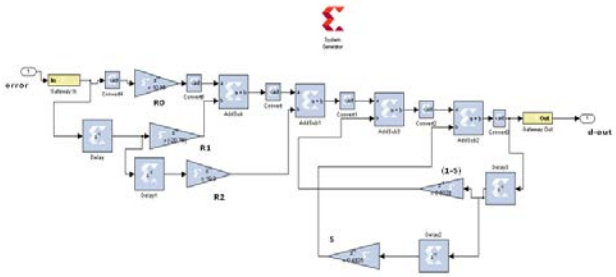

Fig. 5 PID Controller Implementation through XSG

In order to perform the hardware co-simulation to validate the design operating on the FPGA platform, Extreme DSP Development Kit is selected as a target device. After the successful generation of VHDL code, a new hardware co-simulation block is automatically created (Fig. 6). A Simulink library is created containing the hardware co-simulation block. The co-simulation block replaces the previously used System Generator simulation blocks. The hardware implementation is then executed by connecting the board to the PC.

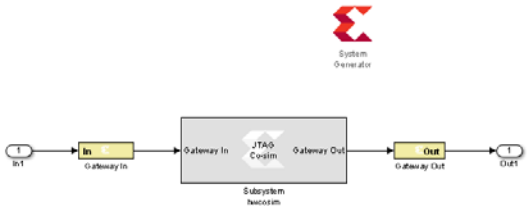

Fig. 8 Hardware Co-Sim block for PID controller

The Xilinx ISE program then generates the bit file and loads it into FPGA through a standard JTAG connection. Further meeting the timing constraints tends to be the most difficult task and is dependent on both the clock frequency and FPGA being utilized. The total path delay introduced by the controller should be less than one clock cycle.

The simulations in System Generator are bit-true and cycle true. Due to this characteristic of XSG, the simulation results look the same as are obtained by the real hardware implementation.

5. Simulation Results

Simulation results obtained by MATLAB/Simulink and are shown in figures from 9 to 12. The performance of the digital control scheme is assessed in terms of time domain specifications associated with output voltage response.
The dynamic response of the system is investigated by changing the load resistance from 5Ω to 3.33Ω. For this change of load, the output voltage settles to its steady-state value within 0.4ms shown in Fig. 9. Fig. 11 depicts that the controller also compensates the perturbations in the supply voltage and thus shows strong line regulation. For a

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reference voltage change of 3V to 4V (Fig. 13), it is seen that the output voltage follows the changes in reference voltage.

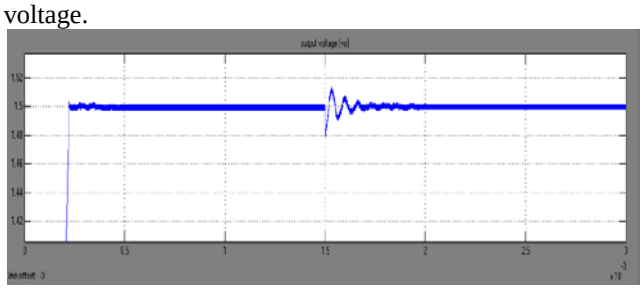

Fig. 9 Output Voltage Response for Change in Load

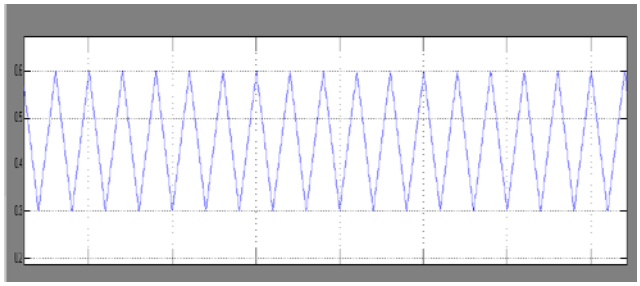

Fig. 10 Inductor Current Ripple for Change in Load

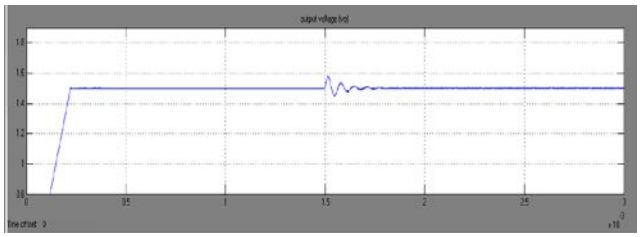

Fig. 11 Output Voltage Response for Change in Supply

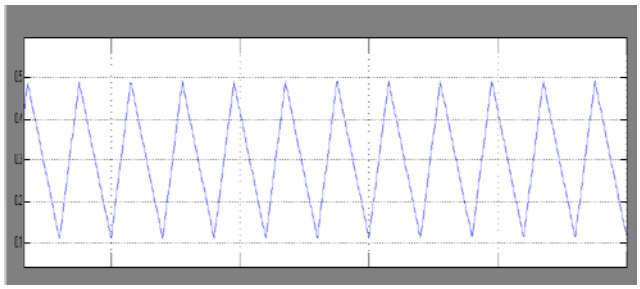

Fig. 12 Inductor Current Ripple for Change in Supply

6. Conclusions

The paper focuses on the faster and easier implementation in Field Programmable Gate Arrays (FPGA) discrete PID controller for the dc-dc buck converter. The XSG is very practical because it does not require the knowledge of any HDL. The availability of XSG blocks and dedicated libraries for implementing advanced control algorithms makes it a highly suitable environment for designing and simulating and implementing the control systems in modern FPGAs with the advantage of being close to real hardware. The implementation technique not only reduces the time of hardware realization but also reduces the cost and uses fewer resources.

Table 1 Comparisons of simulation results

	Load variation at 1.5m sec (0.3A to 0.45A)	**Line variation at 1.5m sec (3V to 4V)**
Closed loop buck converter using Simulink	1.33%(undershoot) 0.3ms(settling time)	5.33%(overshoot) 0.25ms(settling time)
Closed loop buck converter using FPGA	2%(undershoot) 0.4ms(settling time)	12%(overshoot) 0.4ms(settling time)

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