IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 5, July 2014.
www.ijiset.com
ISSN 2348 – 7968

Novel design of Seven Segments Display Unit using FPGA

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Abstract

This Display unit is the most important for any processing unit; so as to display the processed input, output and wired data involved in the manipulation. Liquid Crystal Display unit consists of seven segments has effeciently revolutionized the ancient displaying system. Seven segments are used to display the input data at the input terminal; input as well as the output datum is displayed at the receiver terminal. The input fed into any processing unit is in the form of analog signals and are converted into the digital data and is processed. Then the output data is converted form digital to analog form for diplaying the processed output data. There are various ways to display the data in seven segments Liquid Crystal Display unit in conventional method. Normally the segments in the display unit are attached with the Light Emitting Diode to visualize the segments. In this paper, the seven segments display unit is selected based on the conventional logic gates. The power consumption and the delay of this unit is estimated using the synthsiser 'Xilinx' and is simulated using 'ModelSim'. The delay for the seven segments display unit is about 5.998 ns and the power consumption is estimated to be 151mW at the junction temperature of about 26 deg C.

Keywords: *FPGA, Conventional logic gates, Seven segments display unit.*

.1. Introduction

Every processing unit has certain applications to be performed in them; using the data fed as an input to the unit. Arabic numerals and some alphabets can be display using the seven segment display unit. The seven segment display unit plays a major role in providing the data display effectively when compared to the other display units. The seven segment diaplays are placed almost with equal size in the shape of heoxgons of totally 7 in number; are arranged as shown in fig 1. In the seven segments diaplay unit each and every segment is fixed with the LED's and are made to trigger based on the input voltage fed to the particular segment to be enabled. In this paper, the input to the LED's in the display unit are triggered by switching the form of digital input signal from 0's to 1's using the conventional logic gates. The expression for triggering each and every segment is obtained using the truth table and is simplified for Boolean expressions using K-map. In order to select the particular unit in the seven segments display unit the corresponding logic combinations are to be enabled respectively. The conventional logic gates used for this design implementation are AND, OR, NOT, XOR, XNOR.

2. FPGA

Field Programmable Gate Array (FPGA) is a kit which is made up of several Programmable Logic Arrays. The FPGA enables the implementation of any logic functions with reduced cost, high performance, space and reduced power dissipation. Spartan 3E FPGAs offer the ideal combination of performance and flexibility to address requirements for high resolution, video analytics, and increased channels in vedio surveillance system. The Xilinx tool is used to implement the logic functions effeciently in the Spartan 3E kit.

The power supply required for the FPGA is comparatively very low. It is a programmable analog and digital pheriperals, some control the regulation and load switches in the battery powered system.

In this proposed module the seven segment display unit is performed using the FPGA kit which effectively utilizes low power for the implementation and with minimumm latency [1].

The selection of each and every segment in the display unit is performed digitally. Boolean expression is the simplified form used to perform the logic in the FPGA kit.

3. Seven Segment Display

To implement any display unit, seven segments display unit is the best approach. Seven segment display unit requires very less wiring, low cost and easily available in the market [2].

In this proposed module, the seven segment display unit is implemented by using the Boolean expression so as to reduce the number of gates used. The reduction in the

ISSN 2348 – 7968

number of gates reduces the latency and the power consumption of the display unit.

The seven segments in the display unit are named as A, B, C, D, E, F and G as shown in fig.1. each and every segment in the display unit is attached with the active component LED's which emit light on the particular segment at once the input voltage is fed to the desired segment. In case of the input signal with the desired threshold value is not attained the LED's are turned off. The switching ON and switching OFF of any segment in the display unit is done by feeding 0's (0v) or 1's (threshold voltage to switch ON the LED) at the anode of the LED terminal.

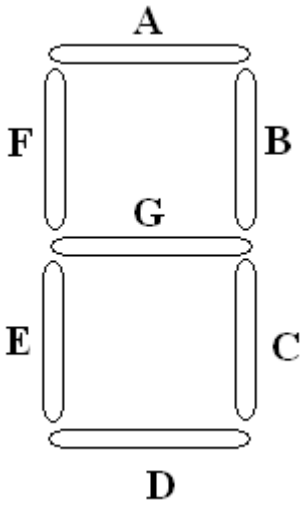

Fig.1 Seven Segments Display Unit.

The conventional logic gates are used to implement the seven segments display unit. The gates used in the implementation are AND, OR, NOT, XOR and XNOR gates with their specific logic to select the desired segment.

The display unit is shown in Fig.1 and their corresponding segment in their Boolean expression representations are given as shown in the fig.2. The respective Boolean logic expressions are given in the Sum Of Product form.

Following logic expression is obtained by solving the Truth table as shown in table 1 using K-map.

INPUT				OUTPUT						
P	Q	R	S	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Table 1.Truth Table for BCD input to Seven Segment Display Unit

K-map effectively reduces the logic gates used which results in the reduced power consumption and latency.

$$A=P+R+(Q \odot S)$$

$$B=\overline{Q}+(R \odot S)$$

$$C=Q+\overline{R}+S$$

$$D=P+\overline{Q}(R+\overline{S})+Q(R \oplus S)$$

$$E=(Q+R)\overline{S}$$

$$F=P+Q(\overline{R}+\overline{S})+\overline{R}\,\overline{S}$$

$$G=P+(Q \oplus R)+Q\overline{S}$$

Fig.2 Logic expression to enable the seven segment display unit.

The corresponding logic has to be selected to enable the desired segment in the seven segment display unit.

The implementation of seven segments display unit has been done using the conventional logic gates and are synthesised using the FPGA kit.

Xilinx synthesiser produces the estimated value of the power dissipation and the latency of the logical implementation.

Selection of each and every segment is performed using the logical expressions. The particular segment is made to switch ON or OFF based on the requirement of the display unit. Each and every segment is in the shape of the hexagons which are equally spaced [3]. The desired segments are selected by enabling the LED's attached to each segments.

The implemetation of the logic gates make the Seven Segment Display unit to be simpler and occupy less space.

ISSN 2348 – 7968

The logic gates operate in the digital form of the input signal they are immune to the noise signal.
The display unit with noise prevents the data from its accuracy which is not appriciated in any application over various fields.
In this proposed module the FPGA kit is used to implement the logic expression so as to enable the logic function; to select the corresponding segments among the seven segments.

5. Result and Discussion

The fig.1 shows the RTL schematic view of the entire proposed module which have been generated using the Xilinx Synthesiser tool.

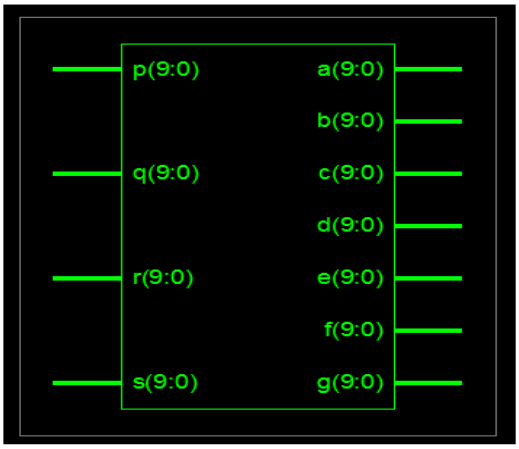

Fig.1 RTL Schematics for seven segments display unit

Resistor Transfer Logic (RTL) is a design abstraction to represent the actual wiring of the digital module. RTL defines the data flow between the logic representation and the hardware register for the coding written in the Hardware Discription Language (HDL) [4] .

This RTL schematic diagram shows the p, q, r, s are the 4-bit input to the seven segments display unit and the outputs are a, b, c, d, e, f, g which selects the segments corresponding to the input data fed in the form of the boolean expression.

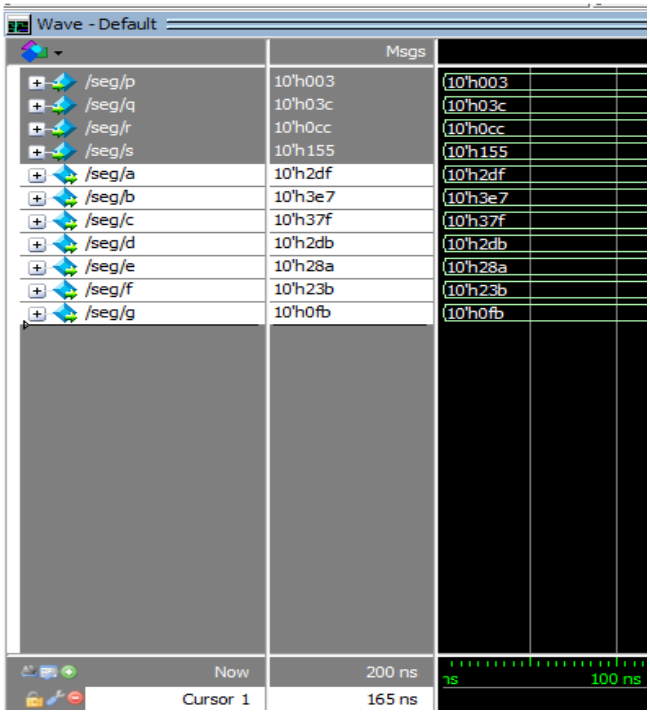

Fig.2 Simulation result of seven segments display unit

The simulation result shows the output for the seven segments display unit which have been simulated using the Modelsim simulator. This simulator result shows the output signal for the seven segments for the input signal combinations fed to the logic module.

Logic Utilization	Used	Available	Utilization
Number of slices	40	4.656	1%
Number of 4 input LUT	70	9.312	1%
Number of bonded IOB's	110	232	47%

Table 2 Synthesis report for Seven segments Display unit.

From the table 1 the utilization factor for the number of slices, number of 4 input Look up Tables and number of bonded IOB's is synthesised using the FPGA kit in the Xilinx Synthesiser.

The power consumption was estimated to about 151mW when the junction temperature of the each Field Effect Transistor is about 26 deg C. The delay for selecting the seven segment display unit is estimated to be 5.998 ns. The delay for this proposed model is about the range of nano seconds; which is comparatively very less. Selection of the segments in the logic design is implemented using the conventional logic gates in the FPGA via the platform of Xilinx Spartan 3E kit.

ISSN 2348 – 7968

4. Conclusions

The seven segments of a display unit have been proposed by using the Boolean expression and is implemented in the FPGA kit in the xilnix synthesiser. In this paper, the power consumption was estimated to be 151mW at the junction temperature of about 26C. The delay in the selection of the segements is about 5.998 ns and is promised to be the high speed model with reduced number of gates to select the seven segments in a display unit. This proposed model streaches the wide range of utility in various fields like space science, signal processing unit, communication, comparators and calculators.

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