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Implementation of 16 bit Arithmetic Logic Unit using Toffoli Reversible logic gate.

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Abstract: Basic logic gates forms the fundamentals of electronic systems. NAND, NOT and NOR are logic gates which is used in realization of logic circuits. Arithmetic logic unit is realized using these gates. In this paper a traditional ALU which was constructed using AND/OR gate is realized using reversible logic gates. The power dissipation in terms of loss of information bits is is reduced significantly when logic gates were replaced by reversible gates. The proposed reversible 16-bit ALU reduces the loss of information bits, and this loss is compensated by reusing the bits and there by the power loss can be reduced.. Simulation of these circuits is done by Mentor graphics tools and language used for programming is very high speed hardware integrated circuit hardware descriptive language, Verilog.
Keywords: Reversible logic gates,Fredkin gate,Tofolli gate,Garbage output,.

1. Introduction

The advancement of reversible logic technologies have helped in improving the performance of computer architectures. Reversible logic is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Significant contributions have been made in the literature towards the design of reversible logic gate structures and arithmetic units. However, there are not many efforts directed towards the design of reversible ALUs. The Binary logic circuits built using traditional irreversible gates inevitably lead to energy dissipation, regardless of the technology used to realize the gates. The power dissipation in any future CMOS will lead to an impossible heat removal problem and thus the speeding-up of CMOS devices will be impossible at some point of time in near future.

According to the theorem of Landauer [1], if we do not consider the factors of technology and material in the manufacture of computer, the energy consumption in computer is mainly produced by the logical irreversible operations. The commonly used gate- AND gate, which has two inputs and one output, one bit lost when the information bits go through this gate. For every bit of information loss, there will generate kT ln2 joules, where k is the Boltzmann's constant and T is the absolute temperature. The generation of heat is inevitable on logic because of the uses of traditional logic gates in computer.

The loss of energy can be minimized or even prevented by applying the principle of reversibility to the operation of digital circuits. It can be shown that for power not to be dissipated, it is necessary to build a circuit from reversible gates. This solution based on the reversible logic promises a circuit operation with arbitrarily small fraction of signal energy. The key point of reversible computing is that the electric charge on the storage cell consisting of transistors is not permitted to flow away when the transistor is switched. Then it can be reused through reversible computing, which can decrease the energy consumption. When there is no loss of information bits, then the system is reversible. In VLSI circuits, it means that the circuits consisting of AND and OR gate, the bit information presented by charge can be saved when it is not used, which leads to the reversibility of the system. Therefore, reversible computing is an appealing solution in many emerging fields such as nanotechnology, as well as quantum and optical computing.

2. THE REVERSIBLE LOGIC GATE

A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one to one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs. Thus the number of inputs and outputs in reversible gates are equal. Any arithmetic logic unit must be able to produce a variety of logic outputs based on inputs determined by the programmer for implementation in an instruction set architecture.

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Therefore, reversible logic devices used in an environment must have both fixed select input lines that receive opcode signals manipulated by the programmer and permanent output lines where the result of the logical output is produced.

For an *n* input/output logic gate, if there is a one-to-one correspondence between its inputs and outputs, then this logic gate is reversible. That is to say, a reversible gate has the same number of inputs and outputs. Commonly used reversible gates are NOT gate, CNOT gate (Feyman gate), Toffoli gate, Fredkin gate and so on.

In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.
- Garbage outputs must be minimum.
- Minimum delay.
- Minimum quantum cost.

Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ (V is square root of NOT gate and V+ is its hermitian) and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2.

V * V = NOT …… (1)

V * V+ = V+ * V = I …… (2)

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates.

2.1. NOT Gate

The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Fig. 1.

Fig.1. Reversible NOT gate

2.2. Feynman / CNOT Gate [8]

The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q= A⊕B) is as shown in the Fig. 2.

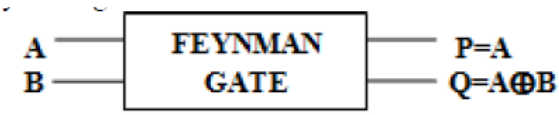

Fig.2. Reversible Feynman/CNOT gate (FG)

2.3. Toffoli Gate [6]

The Reversible 3*3 gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B^C) is as shown in the Fig.3.

Toffoli gate is one of the most popular Reversible gates and has Quantum Cost of 5.

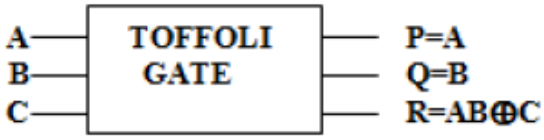

Fig.3. Reversible Toffoli gate (TG)

n -Toffoli gate has *n* intputs and outputs, and the first (n-1) inputs are control bits, the input is target bit Fig. 4. It also can be called the Toffoli gate series.

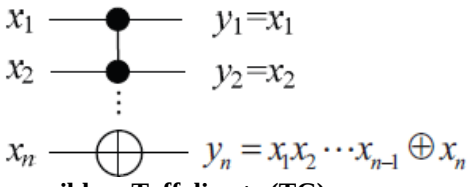

Fig.4. Reversible n-Toffoli gate (TG)

3. THE ARITHMETIC LOGIC UNIT (ALU) BASED ON REVERSIBLE LOGIC GATES

ALU is a data processing component, which is an important part in centre process unit (CPU). Different kinds of computers have different ALUs. But all of the ALUs contain arithmetic unit and logic unit, which are the basic structures. In arithmetic operations there are add, minus, while in logical operations there are NOT, OR, AND, XOR and so on. The above operations can be realized by using reversible logic gates, through which can avoid the energy consumption. The multi-function ALU based on reversible logic gates mainly contains the reversible function generator (FUNC) and the reversible controlled unit (DXOR). The reversible function generator and the reversible controlled unit are cascaded by some *n* -Toffoli gates and NOT gates, and arbitrary bit reversible ALU modules can be realized by this way. In the procedure of cascading the reversible function generator and the reversible controlled unit, we reuse the output signals to reduce the cost of circuit design as much as possible.

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Table 1. The relationship between X_i/Y_i and the control parameters/the inputs

S_0	S_1	Y_i	S_2	S_3	X_i
0	0	$\overline{A_i}$	0	0	1
0	1	$\overline{A_i}B_i$	0	1	$\overline{A_i} + \overline{B_i}$
1	0	$\overline{A_i}\overline{B_i}$	1	0	$\overline{A_i} + B_i$
1	1	0	1	1	$\overline{A_i}$

3.1 The Reversible Function Generator

The function generator"s feature is to process the input information Ai and Bi under the control of the parameters S0, S1, S2 and S3, and then we will get the combined functions Xi and Yi at the output side, where Xi is the combined function on Ai and Bi controlled by the parameters S3 and S2 and Yi is the combined function on Ai and Bi controlled by the parameters S1 and S0.

$$X_i = \overline{S_3 A_i B_i + S_2 A_i \overline{B_i}} \quad (3)$$

$$Y_i = \overline{A_i + S_0 B_i + S_1 \overline{B_i}} \quad (4)$$

According to the above logical expression, the reversible function generator is shown in Figure.5.and its corresponding package diagram is shown in Figure 6.

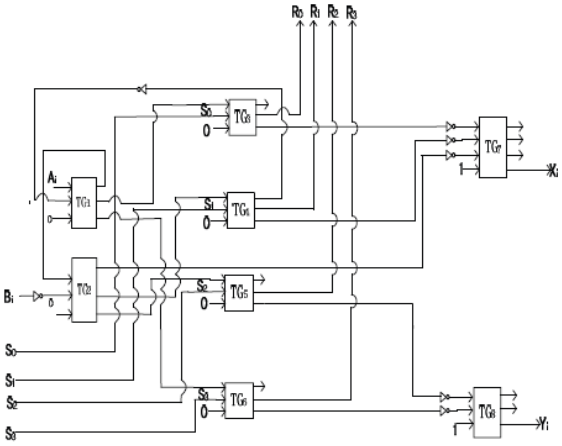

Fig.5.The reversible function generator

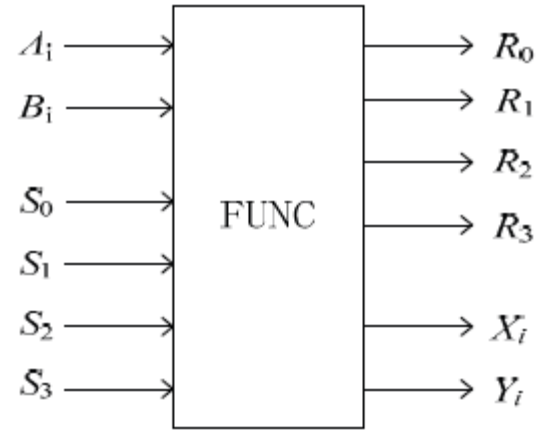

Fig.6.The block diagram of reversible function

3.2 The Reversible Controlled Unit DXOR

The reversible controlled unit DXOR shown in Figure 7 is to complete the sum of the three inputs P, Q and Ci, where P = Xi, Q=Yi. That is to say, let the combined functions Xi and Yi from the reversible function generator add the carry signal Ci to get the final result Fi.

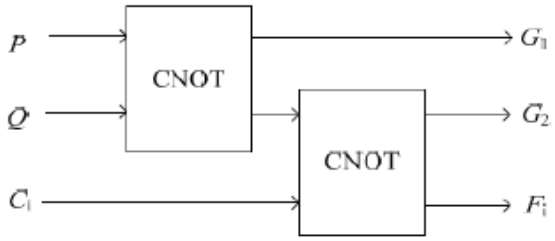

Fig.6. Reversible DXOR

The express of the reversible controlled unit DXOR is: Fi = P ⊕ Q ⊕ Ci ……..(5) where signals *P* and Q come from the reversible function generator's signals Xi and Yi and Ci is the carry signal, Fi is the final output result. The reversible controlled unit DXOR with 3 input/output bits uses two 2*2 Toffoli gates and produces 2 garbage outputs and its corresponding package diagram is shown in Figure 7.

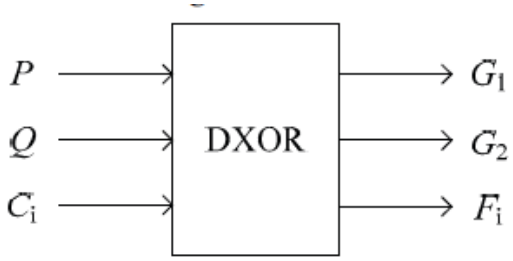

Fig.7.The block diagram of Reversible DXOR

3.3 The Realization of Reversible ALU

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To design the reversible ALU with the minimum cost, we choose 3*3 Toffoli gates and NOT gates to cascade the reversible function generator and the reversible controlled unit. Further, the arbitrary bit reversible ALU modules can be realized through cascading. The reversible ALU in Figure 8 is cascaded by reversible function generators, reversible controlled units and 3*3 Toffoli gates. The reversible ALU performs operations on to binary numbers A = (A7, ……..A0) and B = (B7,……B0).

In Figure 8, the first operand *A*, the second operand *B*, the control signals S0 to S3, the low carry signal Ci and the control signal M are reversible ALU"s input signal, while the result, F = (F7,……..F0) , the carry output signal Cout and the garbage outputs (no letters marked) are the output signals. In addition the outputs R0, R1, R2 and R3 of reversible function generator FUNC0 are respectively seen as the inputs S0, S1, S2 and S3 of reversible function generator FUNC1 and so on. The value of the first and the second inputs of reversible controlled unit DXOR0 – DXOR7 are equal to the value of outputs Xi and Yi of function generator FUNC0 –FUNC7. The value of the third input Ci of reversible controlled unit DXOR0 – DXOR7 have some connection with the control signal M. Their relationship can be expressed as follows:

When i = 0 then

$$C_0 = \overline{C_{in}} + M \qquad \text{.....(5)}$$

When i = 1 then

$$C_1 = \overline{Y_0 + X_0 C_{in}} + M \qquad \text{....(6)}$$

When i>2 then

$$C_i = \overline{Y_i + X_i C_{i-1}} + M \qquad \text{.....(7)}$$

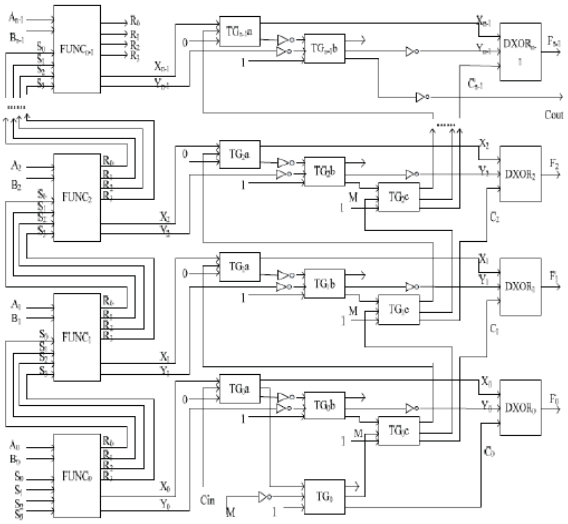

Fig.8.The block diagram of Reversible ALU

The outputs signals Xi and Yi are generated after the input signals Ai, Bi and S0 to S3 passed through the reversible function generator Xi and Yi as the first two input signals of reversible control unit DXORi respectively, and also make operation with control signal M to get the third input signal Ci of reversible control unit DXORi based on the equation 5 to 7.

4. SIMULATION RESULTS

All the blocks of reversible ALU are designed using Verilog HDL (structural form of coding). Verilog code is simulated using mentor graphics using modelsim simulator. The input/ output signals are represented by variables, packaging the variety of Toffoli gates by module, it can be instantiated as the object of Toffoli gate module. The results simulated

Table 2. The function of *n*-bits reversible ALU

Input	Output(F)	
$S_3S_2S_1S_0$	logic operation (M=1)	arithmetic operation (M=0&C_{in}=1)
0 0 0 0	$\overline{A}$	A
0 0 0 1	$\overline{A+B}$	$A+B$
0 0 1 0	$\overline{A}B$	$A+\overline{B}$
0 0 1 1	0	minus 1
0 1 0 0	$\overline{AB}$	A plus $A\overline{B}$
0 1 0 1	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
0 1 1 0	$A \oplus B$	A minus B minus 1
0 1 1 1	$A\overline{B}$	$A\overline{B}$ minus 1
1 0 0 0	$\overline{A}+B$	A plus AB
1 0 0 1	$\overline{A \oplus B}$	A plus B
1 0 1 0	B	$(A+\overline{B})$ plus AB
1 0 1 1	AB	AB minus 1
1 1 0 0	1	A plus A
1 1 0 1	$A+\overline{B}$	$(A+B)$ plus A
1 1 1 0	$A+B$	$(A+\overline{B})$ plus A
1 1 1 1	A	A minus 1

from the programs are same as the results in circuits. So the simulation results can be the base of testing the validation of circuits. Few ALU operations are as shown in the simulation results below.

The figure 9 shows the arithmetic operations.

The Control inputs for these operations are M = '0' and Cin= '1' and output is F and Cout. The Figure 10 shows logical operations. The control inputs for these operations are M = '1' and Cin= '0' and outputs are F and Cout.

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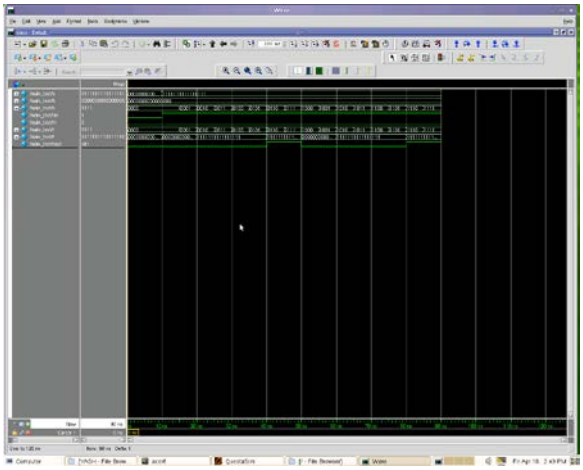

Fig.9. Waveform of Arithmetic operation of reversible ALU

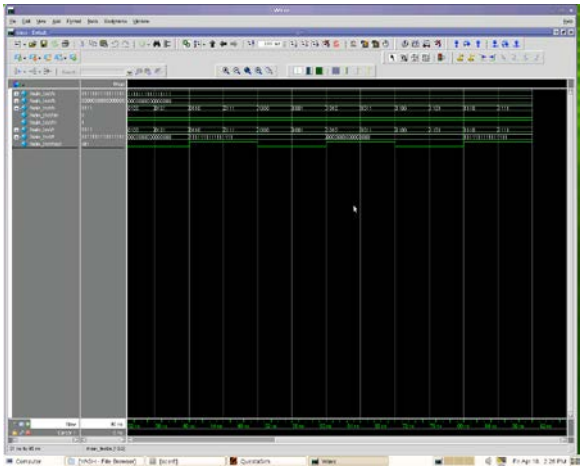

Fig.10. Waveform of Logical operation of reversible ALU

5. CONCLUSION

We have proposed the design and implementation of 16-bit reversible ALU using Toffoli reversible logic gates. The reversibility significantly reduces the use and loss of information bits hence optimal power consumption. The performance checks of various modules are carried out by simulation using mentor graphics. The discussion has focused on logical reversibility-the inputs and outputs that can be uniquely recovered from each other. In future physical reversibility can also be analyzed which is related to the key issue as to whether we can build physical gates and circuits that can actually operate backward and dissipate almost zero power.

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