IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 9, November 2014.
www.ijiset.com
ISSN 2348 – 7968

Analog Phase Lock Loop using CMOS Ring Oscillator in 22 nm Technology

[1]Abhishek Singh, [2] Kalpita Agrawal, [3]Anshita Gupta

Abstract: The Phase Locked Loop is a versatile device which founds its application in many analog and digital electronic devices. In this research paper, we aim at designing a schematic layout of Type I PLL in 22 nanometre process parameter using Microwind 3.1. The VCO used is generating 2.8 GHz frequency and is providing the feedback to phase detector circuit. The PLL designed is generating 1.8-2.8 GHz frequency with reference signal of 2.4 GHz and a clock of more than 120 MHz

Keywords: 22 nanometre, Microwind, Phase Locked Loop, Type I, VCO

1.1 Introduction

PLL means *'Phase-Locked Loop'* and is a closed loop frequency control system, whose performance is based on the detecting the phase between the input and output signals of the voltage controlled oscillator.

The circuit has

- ❖ phase detector (sometimes called phase comparator)
- ❖ loop filter, and,
- ❖ voltage controlled oscillator (VCO) connected in a simple feedback arrangement

The loop is then in a stable equilibrium so that the VCO phase is locked to the input signal phase, $f_o = Nf_i$.

Let us discuss the importance of different blocks of Phase Locked Loop in brief:

Phase detector (PD):

• Analog multiplier

• PD produces a difference signal that is proportional to the phase error, i.e., to the difference between the phases of input and output signals of the phase-locked loop

Loop filter:

• Low-pass filter

• It is characterized by its transfer function F(s)

• Low-pass filter suppresses the noise and unwanted PD outputs. It determines the dynamics of phase-locked loop

Voltage-controlled oscillator (VCO):

• VCO generates a sinusoidal signal

• The instantaneous VCO frequency is controlled by its input voltage

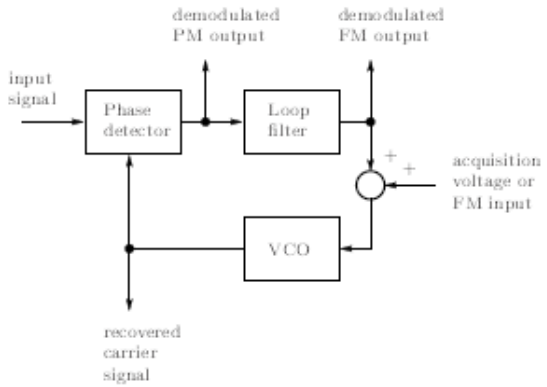

Figure 1: Block diagram Of Phase Locked Loop

1.2 Working of Phase Locked Loop

Phase detector (PD) compares the phase of the input signal against the phase of the VCO output and produces an error signal.

This error signal is then filtered; in order to remove noise and other unwanted components of the input spectrum

The sum of filter output and an additive external control voltage controls the instantaneous VCO frequency.

In every application, the PLL tracks the phase of the input signal. However, before a PLL can track, it must first reach the phase-locked condition In general, the VCO centre

ISSN 2348 – 7968

frequency differs from the frequency of the input signal

Therefore, first the VCO frequency has to be tuned to the input frequency by the loop. This process is called frequency pull-in.

Then the VCO phase has to be adjusted according to the input phase. This process is known as phase lock-in

Both the frequency pull-in and phase lock-in processes are parts of acquisition which is a highly nonlinear process and is very hard to analyze.

After acquisition the PLL achieves the phase-locked condition, where the PLL tracks the input phase. Under this phase-locked condition, the VCO frequency is equal to the input frequency.

1.3 Designing Parameters and Simulation Results

The phase detector we are using is an XOR modulo-2- operator, designed by using transmission gates in 22 nanometre process parameter. It generates the phase difference of incoming signal compared with the feedback signal provided by VCO. The output is then fed to a LPF.

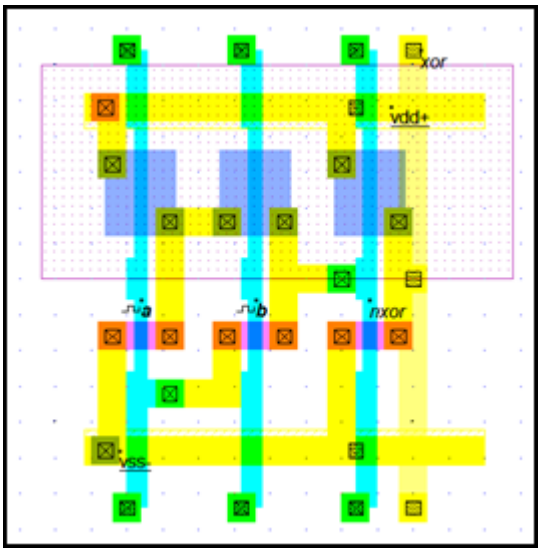

Figure 1.2 CMOS XOR Gate Layout in 22 nanometer Process Parameter

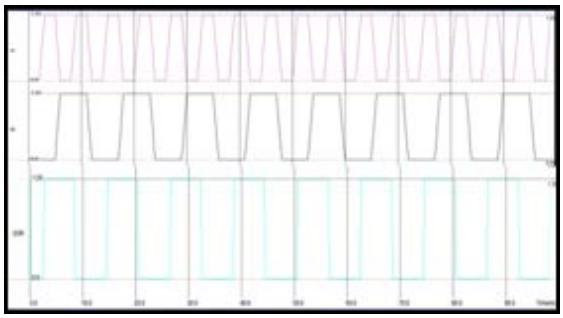

Figure 1.3 CMOS XOR Gate Input and Output Waveforms in 22 nanometer Process Parameter

The Low pass filter is designed by using NMOS. 0.3 pF capacitor acts as load for this filter which is fed as input to Voltage Controlled Oscillator. The phase detector output is connected with low pass filter using a 1000 ohms resistor. RC network have the values as:

R- 5000 ohms

C= 0.3pF

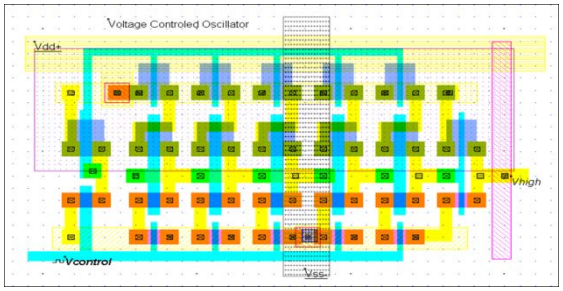

Figure 1.4 CMOS Voltage Controlled Oscillator in 22 nanometer Process Parameter

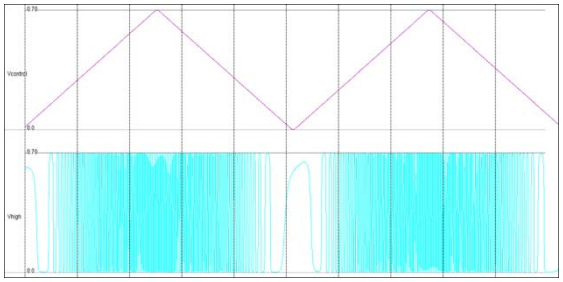

Figure 1.5 CMOS Voltage Controlled Oscillator Input and Output Waveforms in 22 nanometer Process Parameter

The Voltage Controlled Oscillator is designed by using ring oscillator of 7 stages. Ring oscillator is simple to construct and operate using CMOS, as inverter having its basic element. The output of ring oscillator is a 2.4 GHz signal which is fed back to the phase

ISSN 2348 – 7968

detector. 22 nanometre design constraints that we used are as follows:

V_{DD}= 0.7 volts

The W/L parameters for 22 nm PLL is as follows

MOS	W (µ)	L ((µ)	MOS	W (µ)	L ((µ)
N1	0.090	0.020	**P1**	0.150	0.020
N2	0.060	0.020	**P2**	0.150	0.020
N3	0.060	0.040	**P3**	0.140	0.040
N4	0.080	0.020	**P4**	0.150	0.020
N5	0.060	0.040	**P5**	0.140	0.040
N6	0.080	0.020	**P6**	0.150	0.020
N7	0.060	0.040	**P7**	0.140	0.040
N8	0.080	0.020	**P8**	0.150	0.020
N9	0.060	0.040	**P9**	0.140	0.040
N10	0.080	0.020	**P10**	0.150	0.020
N11	0.060	0.040	**P11**	0.140	0.040
N12	0.060	0.040	**P12**	0.150	0.040
N13	0.100	0.030	**P13**	0.090	0.280
N14	0.070	0.280	**P14**	0.120	0.020
N15	0.040	0.020	**P15**	0.120	0.020
N16	0.040	0.020			

The final layout of Phase Locked Loop using 22 nanometre process parameter with its input and output waveforms are as follows:

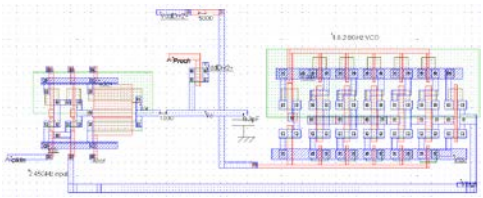

Figure 1.6 Phase Locked Loop in 22 nanometer Process Parameter

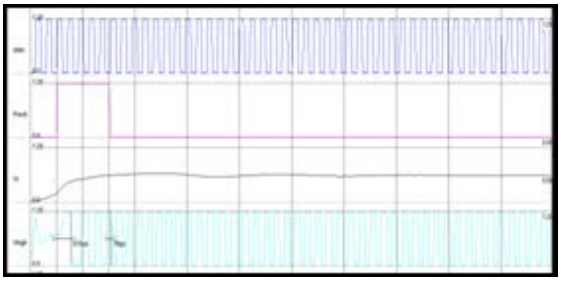

Figure 1.7 Phase Locked Loop Input and Output Waveforms in 22 nanometer Process Parameter

Conclusion

In conclusion, the PLL has been designed block by block and simulated using Microwind 3.1 for layout and schematic simulation. It has been shown that the initial design criterion is achieved by generating a clock signal above 120MHz using the reference signal of 2.4 GHz. The overall design has been achieved in 22 nanometer process technology which is the latest available technology.

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Abhishek Singh is currently working as Assistant Professor in GGITS, Jabalpur. He has a teaching experience of 3 years. He did his Bachelor of Engineering in Electronics and Communication. He did his M. Tech from the same institute in Embedded System and VLSI Design. His area of interest includes Electronics, VLSI and Analog Communication.

Kalpita Agrawal is currently a final year student in GGITS, Jabalpur. She is pursuing her Bachelor of Engineering in Electronics and Communication. Her area of interest includes Electronics, VLSI, Digital electronics and Optical Communication.

Anshita Gupta is currently a final year student in GGITS, Jabalpur. She is pursuing her Bachelor of Engineering in Electronics and Communication. Her area of interest includes Electronics, Digital electronics and Optical Communication.