

# Design of a Low Power 2 – Bit Magnitude Comparator using Full Adder

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**ABSTRACT:** Now-a-days low power circuits have become a top priority in modern VLSI design. This paper presents the power consumption comparisons of various designs of 2 Bit Magnitude comparator. Comparison is the most basic arithmetic operation that determines whether the number is greater than, or equal to or less than the other number. The Existing method uses four different methods of designing a 2 Bit Magnitude comparator such as Pseudo NMOS logic, CMOS logic, Transmission gate logic and Pass Transistor logic. The proposed method uses full adder based design of 2 – Bit Magnitude Comparator. The Full adder is designed using two methods: The First method uses two XNOR gates and one MUX and the second method uses 9T full adder design. The proposed method design demonstrates its superiority against existing 2 Bit Magnitude comparator design in terms of power consumption and transistor count. The Comparison between different designs is calculated by simulation that is performed at 125nm technology in Tanner EDA Tool.

**KEYWORDS:** Binary Comparator, Digital Arithmetic, Full Adder, Low Power, Less Transistor Count.

## I. INTRODUCTION

A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals and one binary digital output. For the 2 – Bit Magnitude Comparator it has two inputs A and B each of two bits. There are three outputs A=B, A>B and A<B. When the input bits A is equal to the input bits of B, then the output A=B becomes 1. When the input bits of A is greater than the input bits of B, then the output A>B becomes 1. When the input bits of A is less than the input bits of B, then the output A<B becomes 1. Any one of the output is always 1.

The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, .... An, etc) against that of a constant or unknown value such as B (B1, B2, B3, .... Bn, etc) and produce an output condition or flag depending upon the result of the comparison.

## II. SYSTEM ARCHITECTURE

The new system is designed such that only two full adders and one AND gate and two inverters are required to build the circuit. The full adder is designed by using two methods: 1. XNOR and MUX based full adder. 2. 9T full adder. The power consumption is much concentrated in this design and is compared for both the methods. This full adder based comparator design uses only less number of transistors and hence the circuit is easier than the existing methods available.

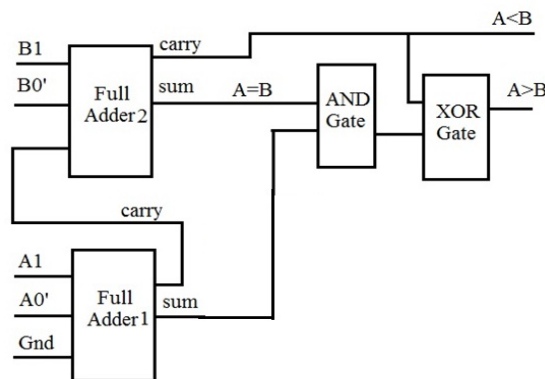


Fig. 1. Block Diagram of Full Adder Based Comparator Design

The above Fig. 1. shows the block diagram for the Full Adder Based Comparator Design. Here three outputs A=B, A>B and A<B is analyzed. When A is equal to B, the output of A=B becomes high. When A is less than B, the output of A<B becomes high. When A is greater than B, the output of A>B becomes high.

### III. SYSTEM DESIGN

The logic diagram for the proposed method is shown in the Fig. 2. below:

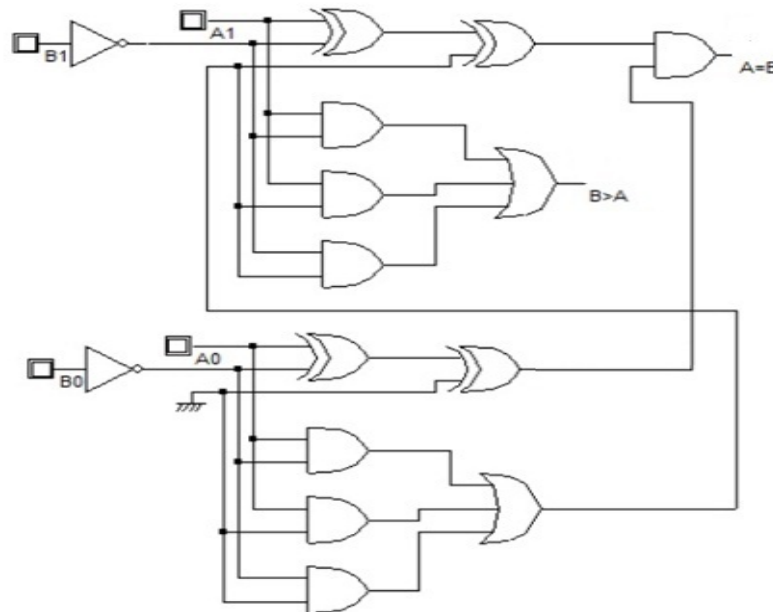


Fig. 2. Logic Diagram of Full Adder Based Comparator

The A>B output is obtained from the above diagram by giving B>A and A=B terminal as input to NOR gate. The output of the NOR gate gives A>B output. The XNOR cell is designed using only 3 transistors as shown in the Fig. 3. below:

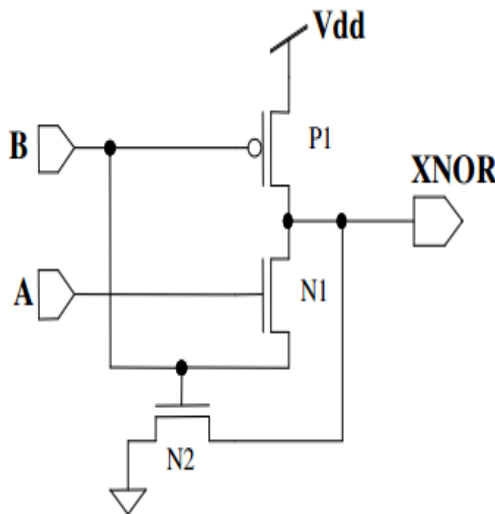


Fig. 3. Circuit Diagram for 3T XNOR Cell

When A=1 and B=0 both transistors (P1 & N1) are on and output node is discharged rapidly by N1 and N2 transistors. In this case with A=1 transistor N1 turns on which further turn on the transistor N2 and a conducting path is provided by N1 and N2. This connectivity of output node with ground discharges the output node.

Due to on condition of transistor N1 the gate voltage of N2 increase above its threshold voltage and transistor N2 also goes in on condition. In this position the circuit is just behaving like an inverter with A=1 as input and gives output as low logic. Transistor P1 is just acting as load resistance with grounded gate input (B= 0). Here the full adder based comparator circuit has been implemented by two 3T XNOR gates and one multiplexer block in full adder designing as shown in the Fig. 4. below:

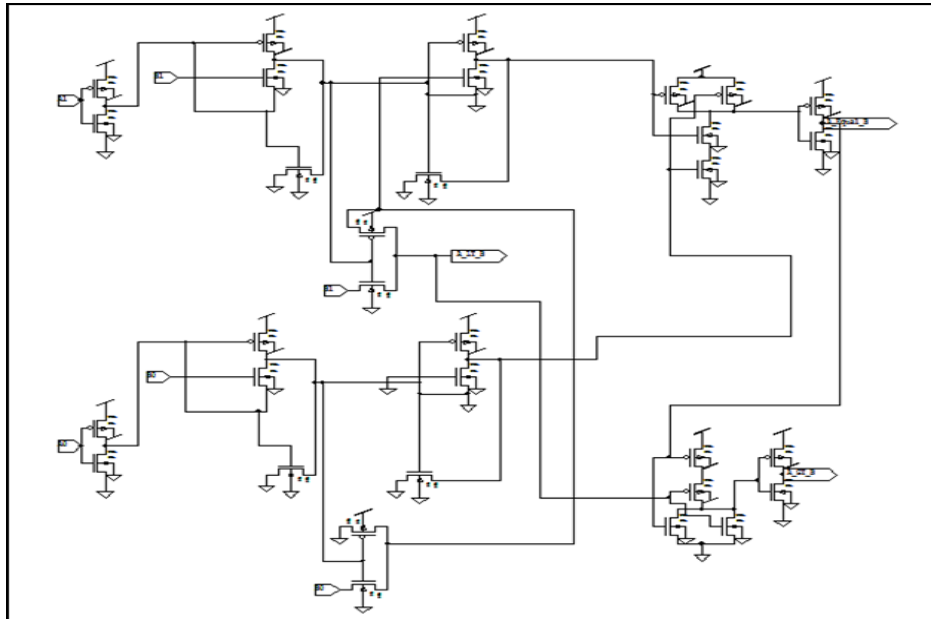


Fig. 4. Schematic Diagram of XNOR and MUX Full Adder Based Comparator

Sum is generated by two XNOR gates and Cout is generated by two transistors multiplexer block. The single bit full adder using proposed XNOR gates with eight transistors has been implemented.

The 9T full adder circuit has reduced power consumption and remains constant with increasing input and supply voltages. All the substrate terminals are connected to their respective source terminals in order to nullify the substrate-bias effect. The Schematic Diagram for the 9T Full adder is shown in the Fig 5. below:

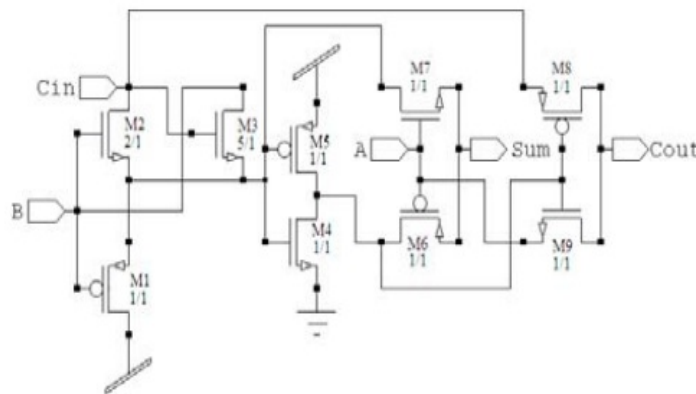


Fig. 5. Circuit Diagram for 9T Full Adder Design

Here the Full adder based comparator circuit has been implemented by 9T logic as shown in the Fig. 6. below. For generating the Sum output in the proposed full adder design, the truth table has been divided into two parts, one for input A='0' and another for A= '1'.

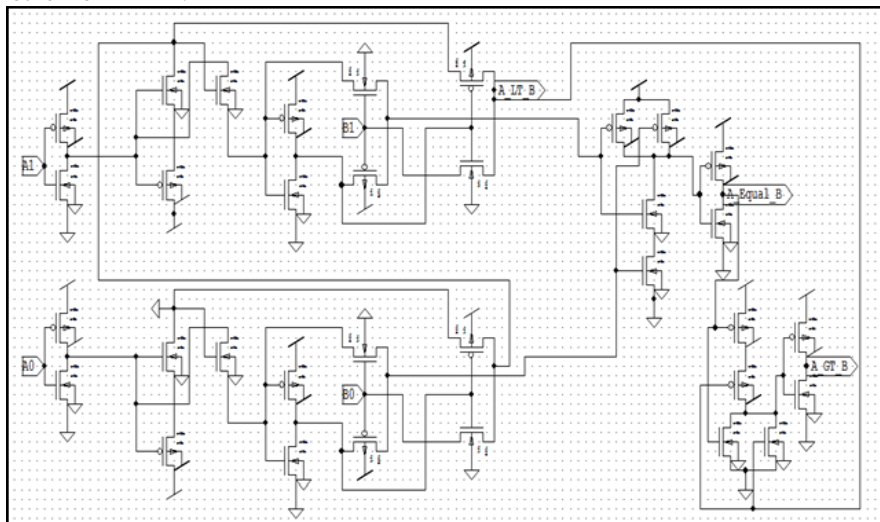


Fig. 6. Schematic Diagram of 9T Full Adder Based Comparator

When A= '0', Sum can be produced by XORing inputs B and Cin. Similarly, when A= '1', Sum is showing the XNORing between inputs B and Cin. Therefore, the operation of Sum module is based on implementing XOR operation and XNOR operation between inputs B and Cin. An inverter is connected at the output of first stage XNOR gate to generate XOR function. Finally the Sum is implemented by transferring these output levels through 2T multiplexer. This 2T multiplexer is controlled by input A. Cout is implemented by using another 2T multiplexer which is controlled by output of first stage XNOR gate and passes either A or Cin accordingly.

#### IV. EXPERIMENTAL RESULTS

All schematic simulations are performed on Tanner EDA tool version 7.0 at 125nm technology with supply voltage 5 V.

The input and output waveform for the XNOR and MUX full adder based comparator is shown in the Fig. 7. below:

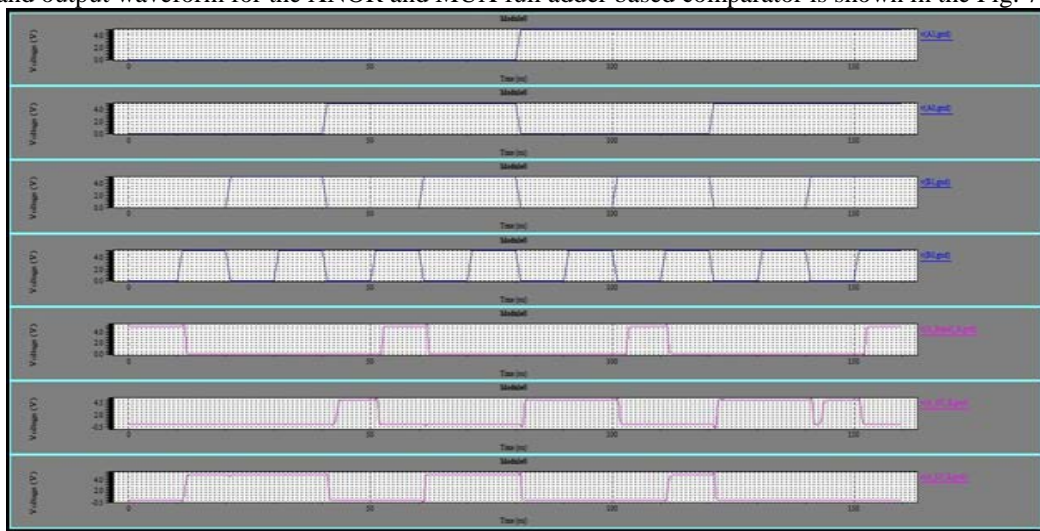


Fig. 7. Input and Output Waveform for XNOR and MUX Full Adder Based Comparator

The input and output waveform for the 9T full adder based comparator is shown in the Fig. 8. below:

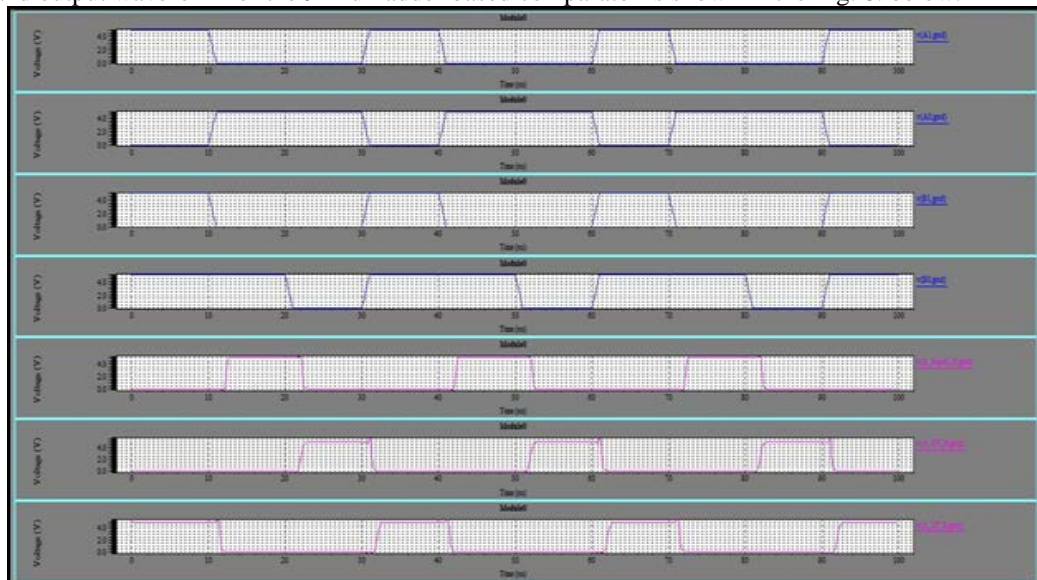


Fig. 8. Input and Output Waveform for 9T Full Adder Based Comparator

TABLE I shows the Transistor Count and Power Consumption Comparison for various logics:

TABLE I Performance Comparison

Logic	Transistor count	Power consumption in watts (For Input supply voltage 5V)
XNOR and MUX Full adder based Comparator	32	3.006801e-002
9T Full adder based Comparator	34	2.000509e-002

## V. CONCLUSION

In this project we have developed a Full adder based comparator which consumes less power than the other methods of design. XNOR and MUX full adder based comparator uses less number of transistors than the other logics as well as 9T full adder based comparator. The power consumption is less in 9T full adder based comparator than other logics as well as XNOR and MUX full adder based comparator.

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