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Design of Digital Down Converter (DDC) for GSM

[1]Jasmine. S and [2]R.Latha

[1] Department of Electronics and Communication Engineering, Faculty of Engineering- Christ University, Bangalore, Karnataka, 560060, India

[2] Associate Professor, Department of Electronics and Communication Engineering, Faculty of Engineering-Christ University, Bangalore, Karnataka, 560060, India

Abstract

In this paper the programmable Digital Down Converter (DDC) structure is proposed which can be used in digital receivers that meets GSM specifications in wireless communications systems. The major advantage of the proposed DDC is that it does not have the passband drop which is very often associated with the Cascaded Integrator-Comb (CIC) based DDCs. Another improvement of the proposed DDC structure compared to the existing off-the-shelf DDC products is that, instead of operating at the input (high) sample rate, the multiplications of the quadrature mixing process are performed at a much lower sample rate. MATLAB and Xilinx ISE 12.3 version software is used for simulating each block of DDC at system level testing.

Keywords: *Digital Down Converter (DDC), GSM, CIC Filter, Decimation.*

1. Introduction

The basic concept of the Software Defined Radio (SDR) is that the radio can be totally configured or defined by the software so that a common platform can be used across a number of areas and the software used to change the configuration of the radio for the function required at a given time. SDR consists of several components and DDC is used as a heart of SDR application.

In the current scenario, Digital Communication is one of the commonly used modes of communication, due to its advantages over Analog Communication. A Digital Communication system has three basic blocks a transmitter, channel and a receiver. The DDC is the key component of Digital Radio Receiver. Digital Radio receivers often have fast ADC converters to digitize the band limited RF or IF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable.

A Digital down Converter converts a digitized real signal centered at an Intermediate Frequency (IF) to a base banded complex signal centered at zero frequency by using a mixer. Also in addition to down conversion, DDC's typically decimate to a lower sampling rate by using several stages of decimation filters.

DDC is a technique which takes band limited high sampling rate digitized signal, shifts the band of interest to a lower frequency and reduces the sample rate while retaining all the information. Though simple and multiplierless, CIC filters suffer from non-flatness in the passband (high passband drop). This is particularly true when the information bandwidth is not very narrow (relative to the sampling rate) or the order of the CIC filter is high. To improve the passband characteristics and overcome the passband drop of the CIC filter, a compensation filter is often required after the CIC filter.Before decimation, filtering is performed using linear phase filters to limit the bandwidth to our signal of interest.

The decimated signal, with a lower data rate, is easier to process on a low speed DSP processor. In a Communication system, the received signals are of high data rates making it difficult to process the signals to extract information of interest. So to solve this problem DDC makes a better solution.

2. Digital Down Converter

The block diagram of Digital Down Converter is shown in Fig. 1.

DDC consists of five basic blocks.

i. *NCO*
ii. Mixer.
iii. Cascaded Integrator Comb (CIC) filter.
iv. Compensating FIR (CFIR) filter.
v. Programmable FIR (PFIR) filter.

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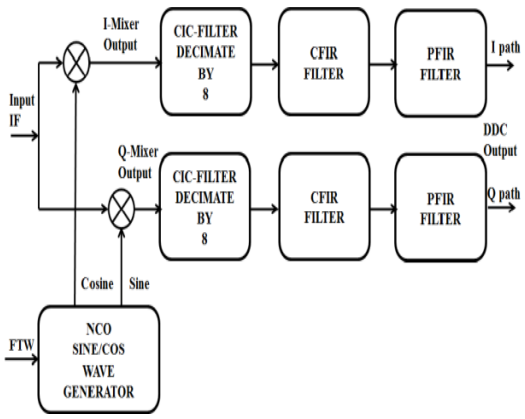

Fig. 1 Block Diagram of DDC

2.1 NCO

A numerically controlled oscillator (NCO) is a digital signal generator creating a synchronous (i.e. clocked), discrete-time, discrete-valued representation of a waveform, usually sinusoidal. Numerically Controlled Oscillators (NCO), also called Direct Digital Synthesizers (DDS), offers several advantages over other types of oscillators in terms of accuracy, stability and reliability. NCOs provide a flexible architecture that enables easy programmability such as on-the-fly frequency/phase.

2.2 Mixer

A mixer is used to convert the IF signal to baseband signal by multiplying the input signal with complex sinusoidal signal cos (wt)-*j* sin(wt) = e^{-jwt} which is generated by NCO thus giving two signals as output i.e.

- i. In-Phase signal
- ii. Quadrature-Phase signal

where these signals are 90 degrees out of phase with each other. The mixer operation is shown in Fig. 2.

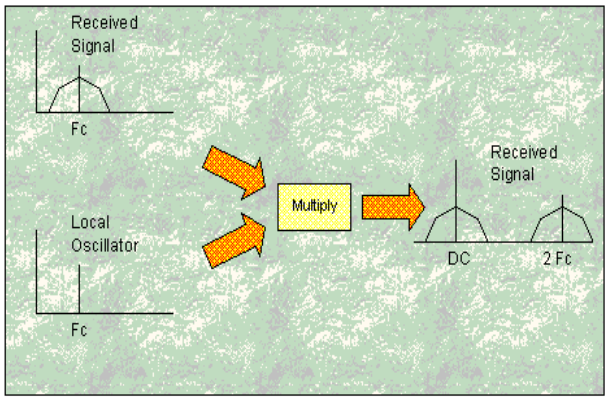

Fig. 2 Mixer operation

2.3 Building blocks of a CIC filter

The cascaded integrator-comb (CIC) filter is a class of hardware-efficient linear phase Finite Impulse Response (FIR) digital filters.

The CIC filter is suitable for this high-speed application because of its ability to achieve high decimation factors and it is implemented using additions and subtractions rather than using multipliers. CIC decimates by R which is programmable.

An integrator: An integrator is simply a single-pole IIR filter with a unity feedback coefficient shown in Eq (1).

$$Y[n] = y[n-1] + x[n] \quad (1)$$

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is given in Eq (2).

$$H_1(Z)=\frac{1}{(1-z^{-1})} \quad (2)$$

Comb Filter (Decimator): A comb filter running at the low sampling rate fs/R is described by Eq (3).

$$Y[n] = x[n] - x[n-RM] \quad (3)$$

A comb filter is a differentiator with a transfer function is shown below in Eq (4).

$$H_c(Z) = 1-Z^{-RM} \quad (4)$$

The transfer function for a CIC filter at f_s is given in Eq (5)

$$H_{cic}(Z) = H_I^N(Z) * H_c^N(Z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \quad (5)$$

Magnitude Response is shown in Eq (6).

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$$H|(f)| = H_1(Z) = \left| \frac{\sin \pi M f}{\sin \frac{\pi f}{R}} \right|^N \quad (6)$$

It is a sinc function which produces unwanted droops in pass band of CIC. To smoothen the pass band characteristics, CIC filter is followed by Compensating FIR (CFIR) filter network.

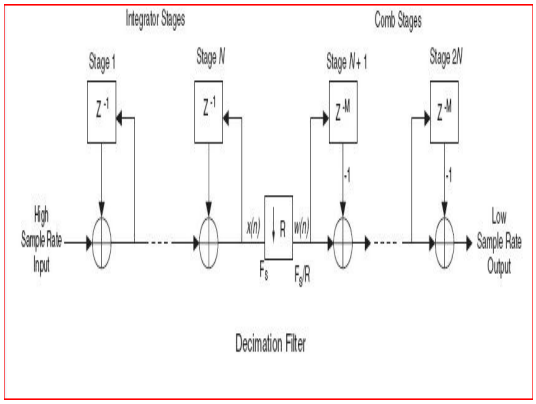

Fig. 3 CIC Filter structure

2.4 Compensation FIR filter

The output of the CIC filter has a sinc shape, which is not suitable for most applications. A "clean-up" filter can be applied at the CIC output to correct for the pass band droop, as well as to achieve the desired cut-off frequency and filter shape. This filter typically decimates by a factor of 2 or 4 to minimize the output sample. This filter will operate at low frequency (f_s/R) to achieve a more efficient hardware solution. Its magnitude response is an inverse-sinc function. Eq (7) represents the magnitude response of CFIR.

$$G(f) = \left| MR \left(\frac{\sin(\frac{\pi f}{R})}{\sin(\pi M f)} \right) \right|^N \approx \left| \left(\frac{\pi M f}{\sin(\pi M f)} \right) \right|^N = |sinc^{-1}(Mf)|^N \quad (7)$$

2.5 Programmable FIR Filter

The Combined filter response of CIC and CFIR filter has a transition band that is too large, due to the large transition band from the CFIR filter. The PFIR filter is intended to be used to do the extra work required to meet the GSM specifications. It is a linear-phase FIR filter consisting of 63 taps.

For the final stage, an equiripple FIR filter is chosen which provides an additional filtering; decimation by 2.The output from Programmable FIR (PFIR) is the final down converted output.

All other characteristics is same as that of CFIR filter except the number of filter coefficients chosen.

3. DDC in GSM and Simulation Results

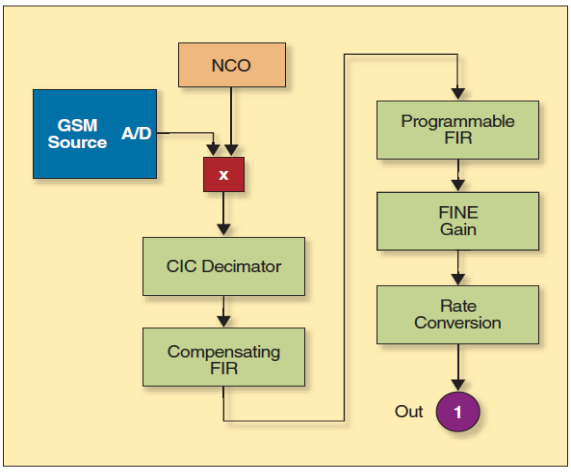

Fig. 4 GSM Digital Down Converter

The block diagram representation of usage of Digital Down Converter in GSM standard is clearly indicated in Fig. 4.

The 5-stage CIC filter takes the high-rate input signal and decimates it by a programmable decimation factor of 64. The CIC filter is followed by a 21-tap CFIR filter that equalizes the "droop" due to the CIC filter and provides further low-pass filtering and decimation by 2.

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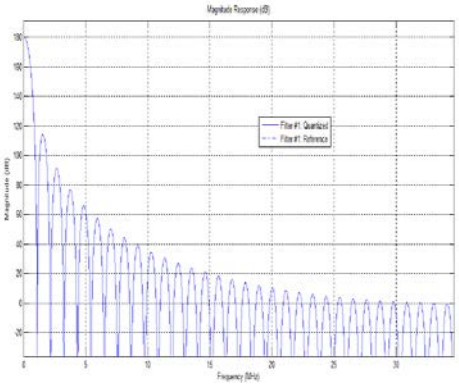

Fig. 5 Magnitude Response of 5 Stage CIC filter

The Magnitude response of 5 stage CIC filter output response is shown in Fig. 5 where they are then followed by CFIR filter. The CFIR is followed by a 63-tap programmable FIR (PFIR) filter that is used for a final decimate-by-2.

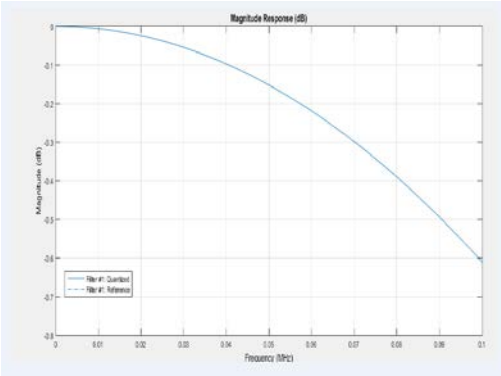

Fig. 6 Pass band details of scaled 5-stage CIC decimator

Since the overall pass band of CIC is desired to be 80 kHz, it is worthwhile to look at the CIC response in this band to get an idea of what the CFIR filter must compensate for. The passband details of the CIC filter are shown in Fig. 6.

The zoomed-in plot of sinc compensation is shown in Fig. 7. The plot covers approximately the band [0.1 kHz]. It is evident from the plot that the combined response is virtually flat in the passband (up to 90 kHz).

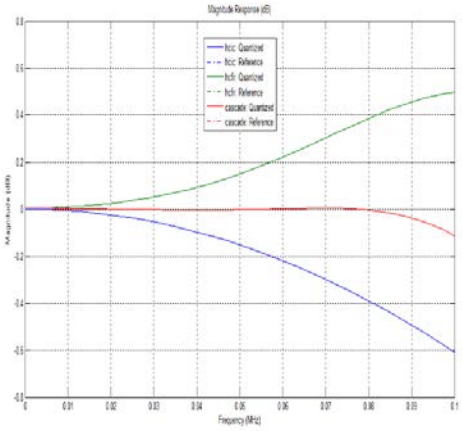

Fig. 7 Pass band details for the magnitude response of CIC filter and CFIR filter overlayed, along with the combined response of the 2

The filter shows a droop with an attenuation of about 0.4 dB at 80 kHz. This is far more than the allowable peak to peak ripple. To see if the overall filter response meets the GSM specifications, we can overlay the GSM spectral mask on the filter response.

To design of an optimal equiripple filter to make the most of the 21 taps available. The overall response of the combination CIC*CFIR*PFIR is shown in Fig 8.

A Programmable Finite Impulse Response (PFIR) in order to shape the GSM mask frequency.We can see that our overall filter response is within the constraints of the GSM spectral mask.

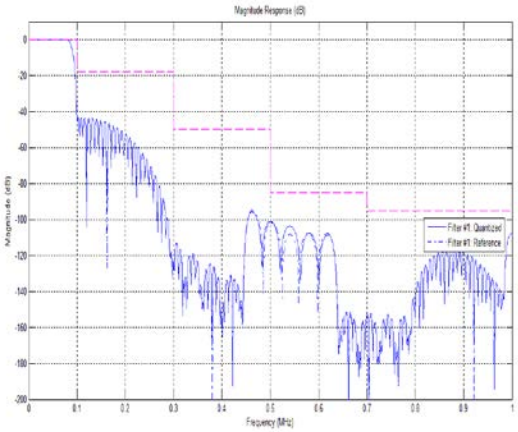

Fig. 8 GSM mask frequency with -0.013db passband ripple.

We also need to ensure that the passband ripple meets the requirement that it is less than 0.1 dB peak-to-peak. We can verify this by zooming in using the axis command.

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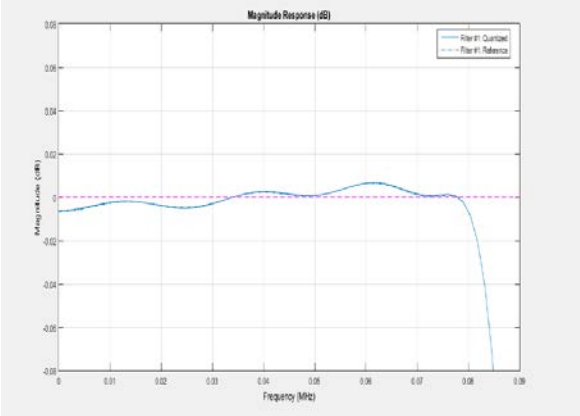

Fig. 9 Peak to Peak ripple less than 0.1dB

The requirement that the peak to peak ripple be less than 0.1 dB is easily met as shown in Fig 9.The GSM spectrum requirement is achieved as illustrated in Fig. 10.

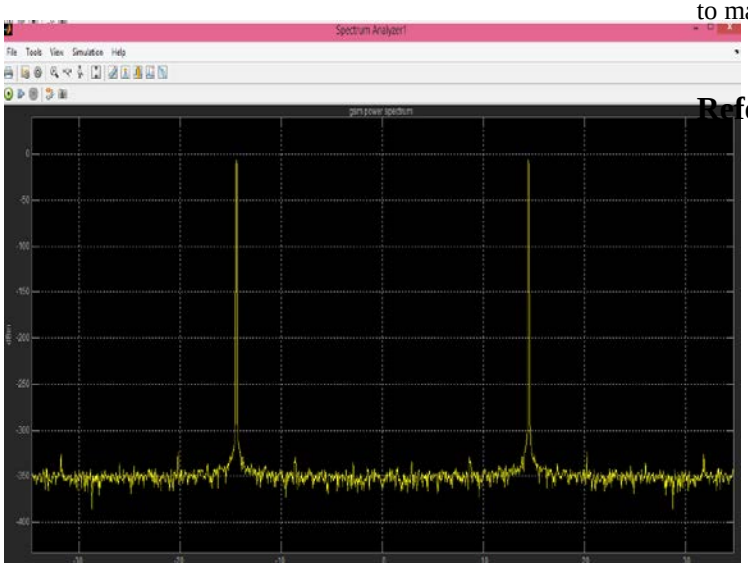

Fig. 10 GSM spectrum produce by proposed filter

4. Conclusions

SDR is a significant technology that will be widely used in 3G and 4G. DDC is one block of SDR, we introduce DDC into the application of GSM base station. A 3 stage DDC module for GSM base station is given based on SDR as a trade-off between number of stages and complexity. To implement this process, two filters namely CFIR and PFIR are used.

For GSM processing, the channel bandwidth of 200 kHz could be extracted from 5MHz received signal and down samples to the original sample rate of 270.833 Kbps by using decomposition of three stages filter. The first stage in this decomposition is the Cascaded Integrated Comb (CIC) filter with down sampled factor of 64 to introduce 270.833 kHz. The GSM requirement will satisfy by adding further filtering stage such as Compensating Finite Impulse Response (CFIR) to reduce the signal rate to 200 kHz. Finely, a Programmable Finite Impulse Response (PFIR) is used to shape the GSM mask frequency. The methodology used to design equiripple FIR filter is simple and leads to good optimal FIR filters with respect to other methods. This technique allows designers to explicitly control the band edge and relative ripple sizes on each band of interest. Also here we compensate the adjacent band rejection and blocker requirements of the filter by moving the passband.

By the computation and simulation, we observe that the simulation results show that the DDC system is feasible and the filters are effective, which makes the development of DDC on GSM more economical and effective and accelerate the transition from academic idea to market place viability.

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Jasmine.S is pursuing M.Tech Communication System at Christ University, Bangalore. Completed Bachelor's degree in Electronics & Communication Engineering under Anna University in the year 2014 and is currently working under Digital Down Converter in GSM, WCDMA.

Prof. R.Latha, M.E, working as an Associate Professor in Electronics and Communication in Faculty of Engineering-Christ University, Bangalore. Completed M.E Graduation from Bharathiar University in the year 2004 and currently undergoing research work in Multirate DSP and VLSI under Anna University, Chennai.