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Reduced Power Consumption Memory Cell with 8T SRAM Cell

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Abstract—Low-power SRAM design is crucial since it takes a large fraction of total power and die area in high-performance processors. Various research works have been done to trim down its power consumption. There are two ways of reducing overall power consumption in CMOS SRAM these are either by decreasing the dynamic power or decreasing standby power. CMOS Technology, power dissipation in cmos circuits, 8T cell is discussed in this paper. The whole circuit verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit.

A. Introduction

In present scenario everyone wants hand held electronics devices with high performance, high speed, long battery life and lot of features. Contemporary society uses all manner of electronic devices built in Automated or semi-automated factories operated by the industry. Our daily lives are significantly affected by electronics, microelectronic technology. Static Random Access Memory (SRAM) is used in high speed applications such as cache memory which is very close or inside the processor and in case of its high power consumption, dissipation of heat generated inside the processor is a problem due to that low power SRAM has become more important. High power dissipation of SRAM reduces the performance and even leads to burnout of IC under some critical conditions. Hence by using low power SRAM we can overcome these problems. Also if total heat generation inside an IC degrades, power budget will also get down and manufacturing cost reduces.

1 Complementary metal–oxide–semiconductor (CMOS)

CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication.

CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field

ISSN 2348 – 7968

effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

2. Power consumption in CMOS

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption. This application report addresses power consumption in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power consumption. Additional information is also presented to help explain the causes of power consumption, and present possible solutions to minimize power consumption in a CMOS system. High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heat sink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency [12].

Two components determine the power consumption in a CMOS circuit:

1. Static power consumption
2. Dynamic power consumption

2.1 Static power consumption

In Static Power Consumption Typically, all low-voltage devices have a CMOS inverter in the input and output stage. If the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON the output voltage is VCC, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from VCC to GND, the resultant quiescent (steady

ISSN 2348 – 7968

state) current is zero. Hence, static power consumption is zero.

2.2.1Sub Threshold leakage current

The leakage current of the diode is described by the following equation

$I = Is(e^{qv/kt}-1)$

Where Is = reverse saturation current

V = diode voltage

k = Boltzmann's constant (1.38×10^{-23} J/K)

q = electronic charge (1.602×10^{-19} C)

T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption can be obtained as:

PS= (leakage current)*(supply voltage)

The leakage current ICC (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or PS, and can be calculated as:

$P_S = V_{CC} * I_{CC}$

Where:

V_{CC} = supply voltage

I_{CC} = current into a device

2.2 Dynamic power consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (PT), and capacitive-load power consumption (PL). It can be of two types: Transient Power Consumption, capacitive-load power consumption

2.2.1Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from VCC to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, has a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is

Governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance. Transient power consumption can be calculated as [12].

$P_T = C_{pd} * V_{cc}^2 * fi * N_{sw}$ …….. (1)

Where

P_T = transient power consumption

V_{CC} = supply voltage

f_I = input signal frequency

N_{SW} = number of bits switching

C_{pd} = dynamic power-dissipation capacitance

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{ap} can be measured with no output switching

ISSN 2348 – 7968

(output disabled) or with any of the outputs switching (output enabled).

B. SRAM OPERATION

Basically, SRAM operations are synchronized with its peripherals and given as data write, read

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C. Conventional 6T CMOS SRAM Cell

The conventional 6T SRAM cell is shown in Fig 1. The cell consists of 4 NMOS and 2 PMOS transistors. Structure can be visualized as two cross-coupled inverters with two NMOS transistors as word select. The write and read operations are:

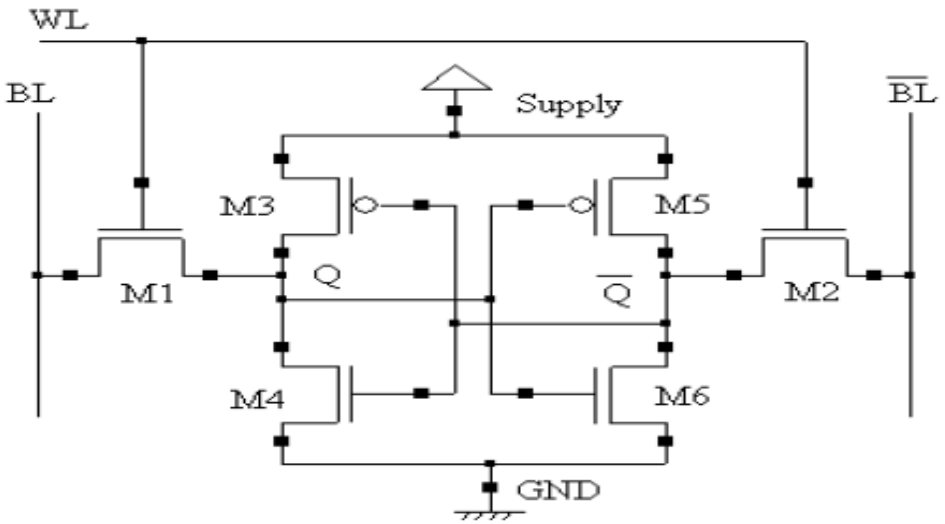

Fig1. Conventional 6T SRAM Cell

D. Low Power SRAM

Figure 2 shows the write mode SRAM. SRAM [13] cell introduced one Control signal transistor for controlling these transistors in this figure. But due to one more transistors area is increased in comparison to Conventional approach. This control transistor uses control select signals which can properly control the dissipation [3] [10] in power.

ISSN 2348 – 7968

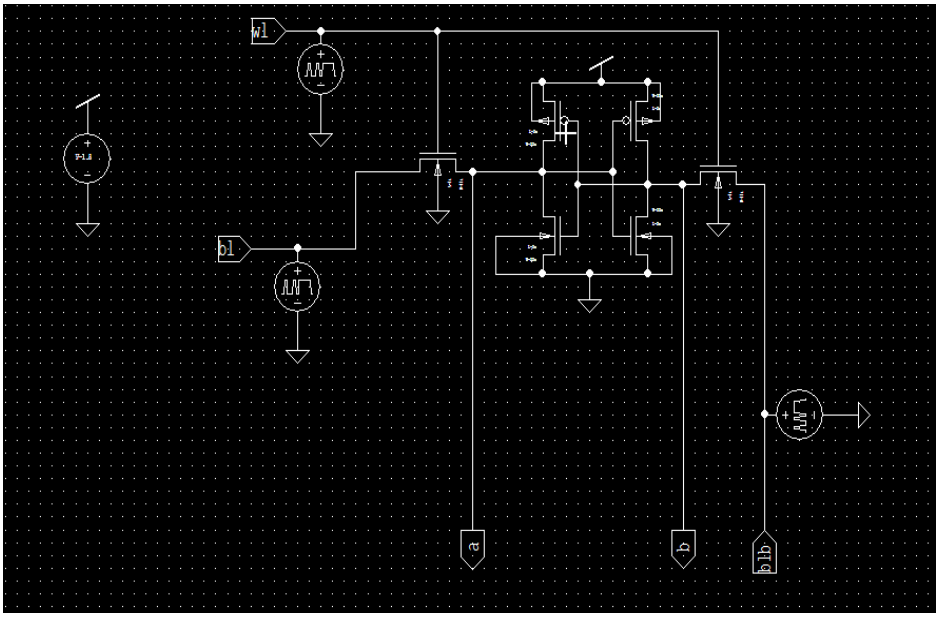

Fig2. Simulated Schematics of 6-T SRAM cell

Figure 3 shows the dual-port cell (8T-cell) created by adding two transistors; the read [11] can be entirely decoupled from the write operation in an 8T [1] cell by sensing the data through a separate read stack controlled by a separate read word lines (RWL).

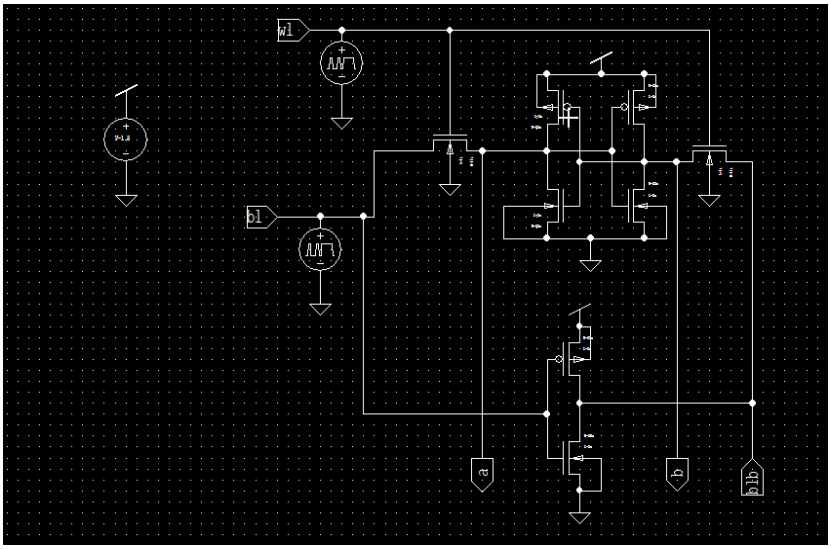

Fig3. Simulated Schematics of Low power 8-T SRAM cell

E. Simulation Analysis

All the circuits have been simulated using 90 nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns.

F. Simulation Results

Figures 4 to 6 shows output waveforms of different SRAM cells at 90nm technology. And the waveform shows the Read/Write Waveforms of SRAM Cell at different technologies. Here v(wl) v(blb) v(bl) are the inputs and v(a) v(b) are the outputs.

ISSN 2348 – 7968

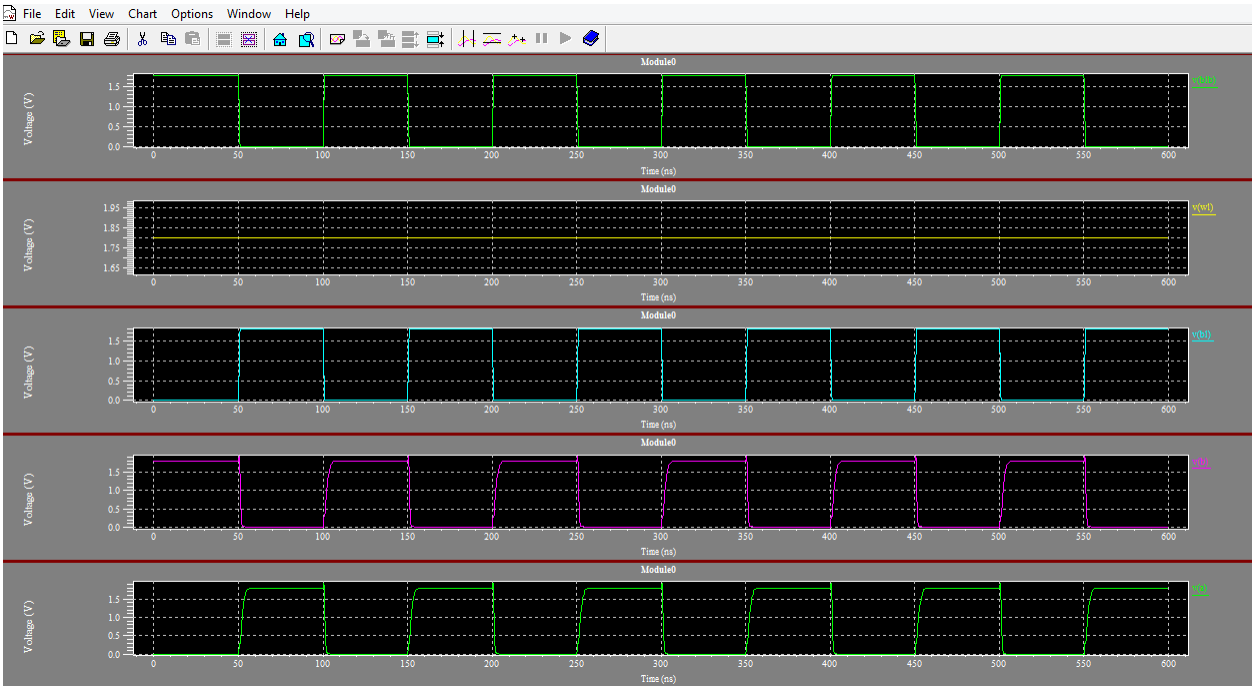

Fig.4 Read/Write Waveforms of 6T SRAM Cell at 90nm

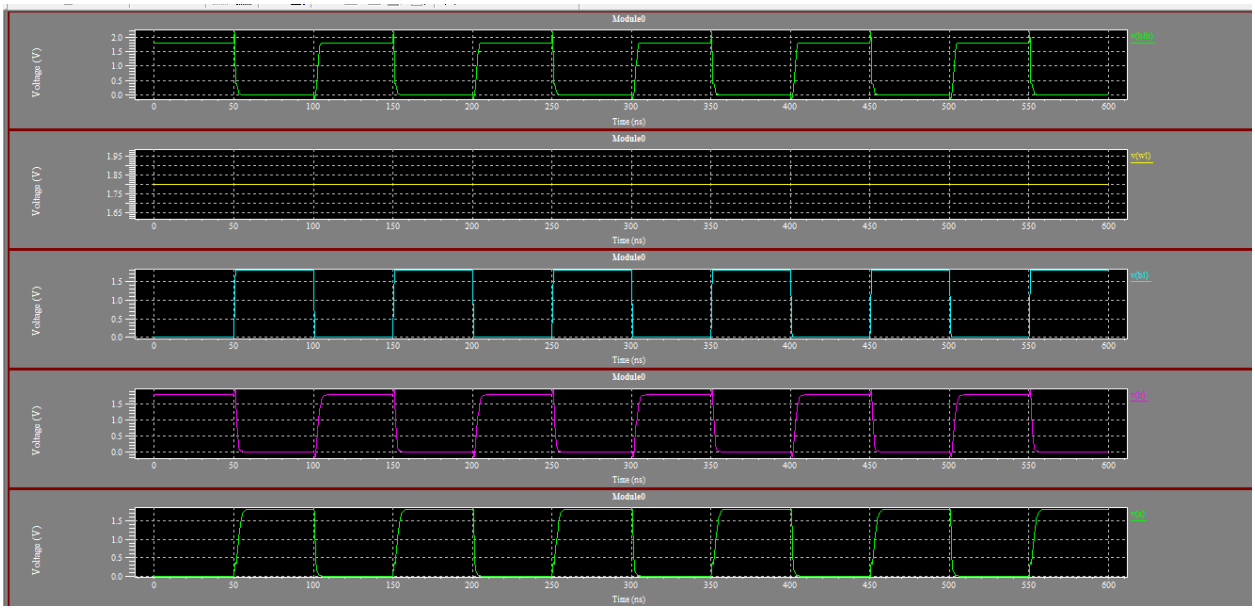

Fig.5 Read/Write Waveforms of 6T SRAM Cell at 90nm

G. Results and Comparative Analysis

All memory cells are simulated using T-SPICE 7.1v. In this section, comparison based results are presented in following tables. These results have been obtained from simulation of 6T and 8T memory cell in asymmetric configuration at the different technologies.

ISSN 2348 – 7968

TABLE 1. Simulation results of 6T SRAM Cell for area, power and delay.

Design style	No. of transistors	Technology file (µm)	Avg. power consumptions(watts)	Prop. delay (a) (sec)	Prop. delay (b) (sec)
SRAM	6	0.90	$9.08x10^{-6}$	$9.22x10^{-9}$	$9.22x10^{-9}$
SRAM	8	0.90	$7.58x10^{-6}$	$11.8x10^{-9}$	$11.4x10^{-9}$

TABLE 2. Simulation results of 6T SRAM Cell for area, power and delay.

Design style	No. of transistors	Technology file (µm)	Avg. power consumptions(watts)	Prop. delay (a) (sec)	Prop. delay (b) (sec)
SRAM	6	0.18	$1.08x10^{-5}$	$8.38x10^{-9}$	$8.38x10^{-9}$
SRAM	8	0.18	$0.99x10^{-5}$	$8.40x10^{-9}$	$8.40x10^{-9}$

Conclusions

The most efficient technique to reduce the power dissipation is the reduction in leakage power. The power dissipation reduction in SRAMs is not only due to power supply voltage reduction, but also due to operating frequency and temperature. Technology scaling demands a decrease in both Vdd and Vt to sustain delay reduction, while restraining active power dissipation. To increase their reliability, the lifetime of battery is a prime concerned at the cost of speed. In this paper the proposed cells utilize single bit line (BL) for write operation resulting in reduction of dynamic power.

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