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Design and Simulation of CMOS Schmitt Trigger

Pranay Kumar Rahi[1], Shashi Dewangan[2], Tanuj Yadav[3], Md Muzaherul Haque[4],
[1,3,4]ME Scholar, [2]Assistant Professor,
[1,3]Department of Electronics & Communication Engineering,
[4]Department of Instrumentation & Control Engineering,
National Institute of Technical Teachers' Training & Research, Chandigarh, UT, India
[3]Department of Physics,
Kamala Nehru College, Korba, Chhattisgarh, India

ABSTRACT

Portable electronic devices have extremely low power requirement to maximize the battery lifetime. Various device circuit architectural level techniques have been implemented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. The Schmitt Trigger is a comparator circuit that incorporates positive feedback. Schmitt triggers are extensively used in digital as well as analog systems to filter out any noise present in a signal line and produce a clean digital signal. The result has been compared in terms of power consumption and required surface area. The 45nm CMOS technology gives better results in terms of power and surface area as compare to 65nm and 90nm CMOS layout of Schmitt trigger. The design and simulation are performed of Schmitt triggers using DSCH and MICROWIND tools.

KEYWORDS: *CMOS, VLSI, Schmitt trigger, Power consumption, CMOS technology.*

I. INTRODUCTION

Traditionally, the goal of CMOS circuit designers has been to obtain the best trade-off between delay and power consumption. As CMOS technology continues to scale towards the nanometer regime, millions of transistors are densely packed to increase the system functionality [8]. In recent years the power is an important parameter in comparison to area and speed [2]. Power consumption is one of the basic constraints in any integrated circuit. There is always a trade-off between power and performance [3]. Power consumption of CMOS consists of dynamic and static components [4]. Dynamic power is consumed when transistors are being switched, and static power is consumed regardless of transistor switching. Modern digital circuit consists of logic gates implement in the CMOS. Dynamic power dissipation is proportional to the square of the supply voltage. In deep submicron process supply voltages and threshold voltages for CMOS transistors have greatly reduced. This reduces the dynamic power dissipation [6]. Sometimes an input signal to a digital circuit doesn't directly fit the description of a digital signal. For various reasons it may have slow rise and/or fall times, or may have acquired some noise that could be sensed by further circuitry. It may even be an analog signal whose frequency we want to measure. All of these conditions, and many others, require a specialized circuit that will "clean up" a signal and force it to true digital shape. The required circuit is called a Schmitt Trigger. It has two possible states just like other multi-vibrators. However, the trigger for this circuit to change states is the input voltage level, rather than a digital pulse. That is, the output state depends on the input level, and will change only as the input crosses a pre-defined threshold. Therefore Schmitt triggers are bi-stable networks that are widely used to enhance the immunity of circuits to noise and disturbances [3].

Schmitt trigger is a circuit with a hysteresis shaped transfer characteristic. Its application is very wide, both in mixed signals circuits and in digital ones. As digital circuits, they are usually referred to as Schmitt logic circuits. Those are circuits with standard elementary logic functions (inverter, NAND and NOR) and a hysteresis shaped transfer characteristic. Because of this, Schmitt logic circuits have larger noise immunity than standard circuits. Schmitt logic circuits are often used to design pulse generators. For example, astable multi-vibrator consists of a Schmitt inverter, a resistor and a capacitor [1]. The block diagram of a Schmitt trigger are shown in fig-1. It is a system with positive feedback in which the output signal feedback into the input to cause the amplifier A to switch from one saturated state to other if the input crosses a threshold value. In the given fig.1, A is the amplifier gain and B is the transfer function [6].

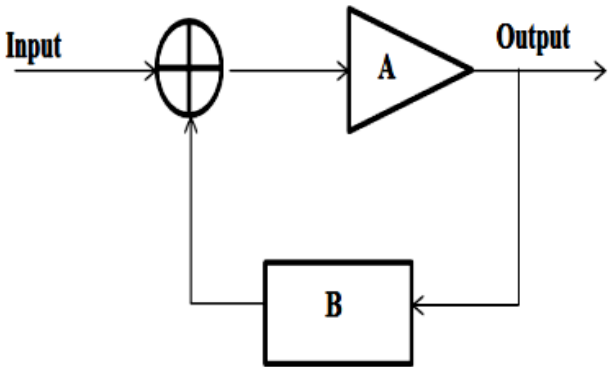

Fig.1: Block diagram of a Schmitt Trigger

II. SCHMITT TRIGGER

The Schmitt Trigger circuit is widely used in analogue and digital circuit to solve the noise problem. Beside that this circuit is widely design in various styles in order to drive the load with fast switching, low power dissipation and low-supply voltage, especially for high capacitive load problem [5]. Schmitt triggers are bistable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as a noise rejecter. Schmitt trigger make use of waves, therefore it is widely used for converting analog signals into digital ones and to reshape sloppy, or distorted re pulses. The output of a Schmitt trigger changes state when a positive going input passes the upper trigger point (UTP) voltage and when negative going input passes the lower trigger point (LTP)voltage[4].

Conventional Schmitt Trigger is shown in Figure 2. where the switching thresholds are dependent on the ratio of NMOS and PMOS. This circuit will exhibit racing phenomena after the transition starts. Therefore in this paper we proposed CMOS Schmitt Trigger circuit which is capable to operate in low voltages (0.8V- 1.5V), less propagation delay. The proposed circuit is formed by a combination of two sub-circuits, P sub-circuit (which consist of P1 and P2) and N sub-circuit (which consist of N1 and N2). There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub- circuit is connected between the path of output and ground. Therefore, there is no static power consumption due to no direct path between source voltage and ground. Two PMOS (P1and P2) are formed by a parallel connection while two NMOS (N1 and N2) are formed by a series connection [7].

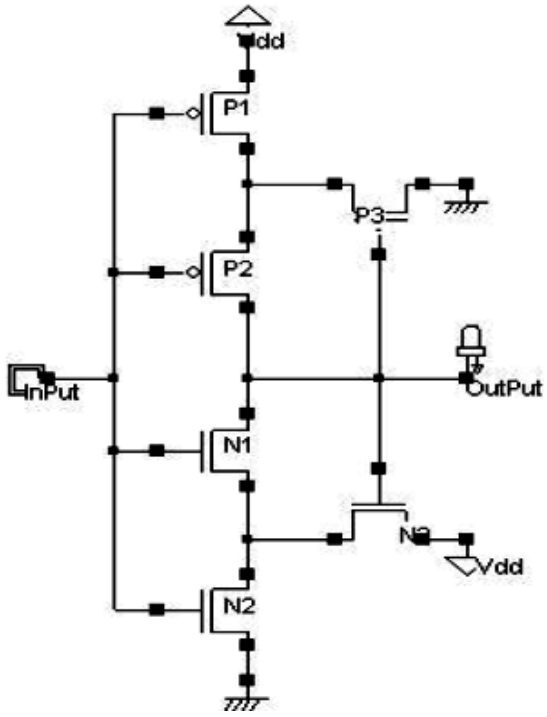

Figure 2.The Conventional Schmitt Trigger

This technique uses aspect ratio for PMOS and NMOS transistor. When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to VDD). During this condition, both P1 and P2 are on (because $V_{gs} < |V_{tp}|$ source voltage and gate voltage is equal). Therefore, the output voltage is pull to VDD. When the input increases to V_{dd}, N1 and N2 is turned on. Thus the output voltage is pull down to GND [8]. This paper demonstrates the power consumption of various models of SRAM cell with feedback mechanism circuit Technique [2].

III. LAYOUT SIMULATION

The proposed schematic circuit is designed and checked by using DSCH software**.** The wire connection is connected and all the parameter such as voltage, width and effective length is settled as shown in Fig. 3 [4]. There are two parts of result. First, functional simulation of Schmitt trigger is using CMOS technology in different foundry. Then, post-layout simulation of Schmitt trigger is done in Microwind 3.1 using 90nm, 65nm and 45nm CMOS technology. The design is implemented using DSCH software to calculate area and power consumption.

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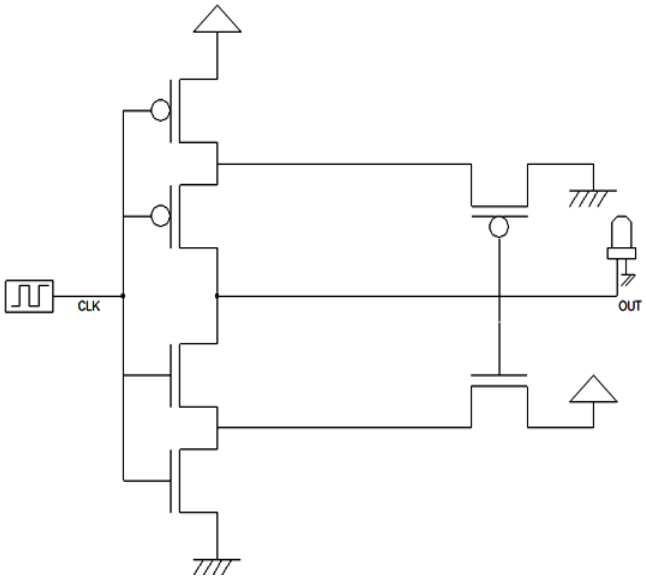

Fig. 4 DSCH schematic design of Schmitt trigger

The designs of CMOS Schmitt trigger is simulated with Micro wind software using different foundry. This paper aims the design to reduce the overall surface area and power consumption such that the design becomes better applicable for the low power applications. The layout design rule describes how the small feature can be and how closely they can be packed in particular manufacturing process. There are specific layers for metal, contacts and diffusion areas and polysilicon.

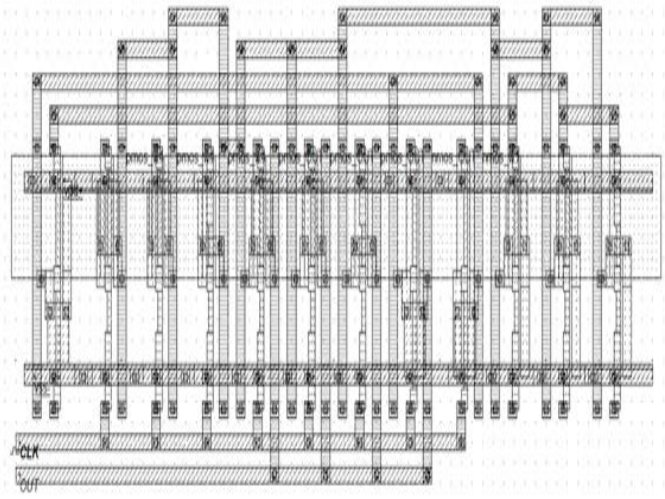

Fig. 5 MICROWIND Layout design of Schmitt trigger

IV. RESULTS

In this paper, the functional and layout simulation results of Schmitt trigger have been proposed. The proposed Schmitt trigger are compared based on the performance parameters *viz* silicon surface area and power requirement. The circuits are designed and simulated using CMOS foundries by Microwind 3.1 in 90nm, 65nm and 45nm technology to achieve better performance. The size of PMOS is twice of size of NMOS. Proposed circuit was designed optimally for speed, power, accuracy and surface area.

The timing diagram results of proposed Schmitt trigger using 90nm, 65nm and 45nm CMOS fabrication technology shown in Figure 6-8.

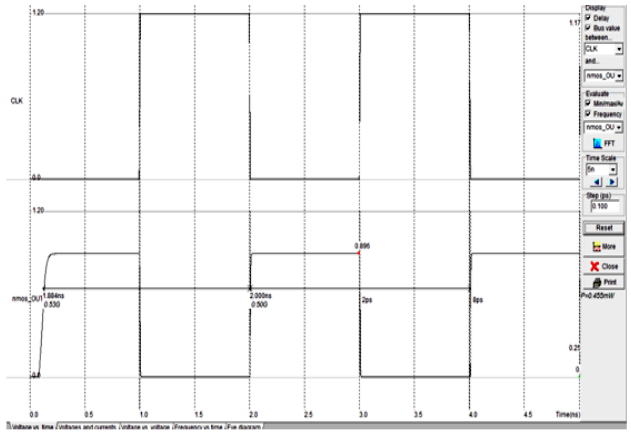

Fig. 6 : Output of Schmitt trigger using 90 nm CMOS Technology

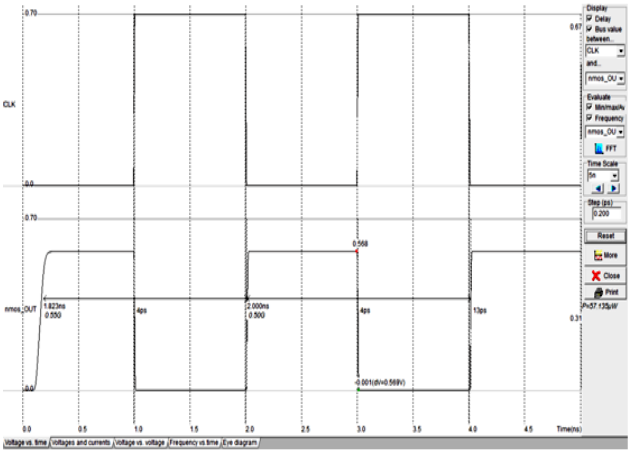

Fig. 7: Output of Schmitt trigger using 65 nm CMOS Technology

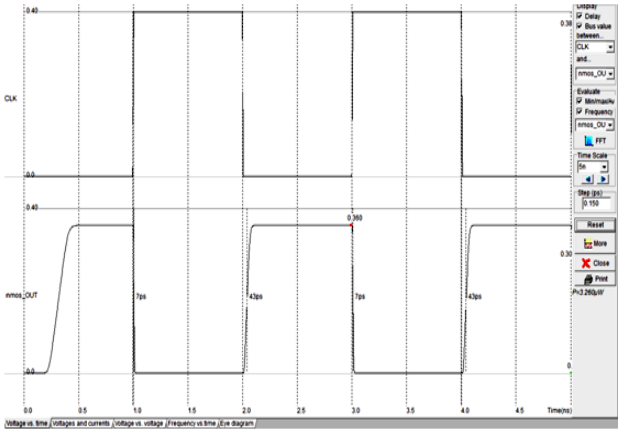

Fig. 8: Output of Schmitt trigger using 45 nm CMOS Technology

The comparative results for proposed Schmitt trigger circuit for 90nm, 65nm and 45nm CMOS design technology are given in Table-2.

Table 2. Power and surface area analysis of Schmitt trigger in different CMOS technologies

CMOS Technology / Parameters	90 nm	65 nm	45 nm
Power (in µW)	455	57.135	3.260
Surface Area (in µm^2)	88.7	43.5	22.2

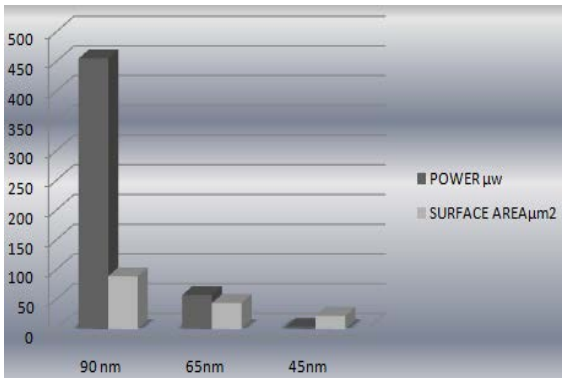

Fig.9: Graphical Comparison of Power and Area

CONCLUSION

In this paper, the proposed Schmitt trigger circuit describes three different designs and their simulation. The 45nm CMOS technology provides low power architecture. The proposed Schmitt trigger design can achieve very low power dissipation and efficient surface area compared with 65nm and 90nm foundry. This method can minimize power consumption and silicon surface area. In VLSI design, a great deal of effort has been made to explore low-power and area design options. The power consumed in 90nm, 65nm and 45nm CMOS technologies are 455µW, 57.135µW and 3.260µW respectively. The silicon surface area required for the Schmitt trigger circuit in 90nm, 65nm and 45nm CMOS technologies are 88.7µm^2, 43.5µm^2, and 22.2µm^2 respectively.

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AUTHORS

Pranay Kumar Rahi received the Bachelors of Technology degree in Electronics and Telecommunication Engineering from Government Engineering College, Guru Ghasidas University, Bilaspur, Chhattisgarh, India in 2004 and pursuing Masters of Engineering in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India. His current research and teaching interests are in Signal and Communications Processing, Communication System. He has authored more than 14 research publications.

Shashi Dewangan received the Bachelors of Science degree from Agrasen Girls College, Korba, Chhattisgarh, India in 2007 and the Masters of Science degree in Physics from Government Science College, Guru Ghasidas University, Bilaspur, India in 2010. She is an Assistant Professor in the Department of Physics, Kamala Nehru College, Korba, India. She has authored more than 7 research publications.

Tanuj Yadav received the Bachelors of Technology degree in Electronics and Communication Engineering from Gautam Buddha Technical Universtity Lucknow, Uttar Pradesh, India in 2010, and pursuing Masters of Engineering in Electronics and Communication Engineering from National Institute of Technical Teacher"s Training & Research, Punjab University, and Chandigarh, India.

Md. Muzaherul Haque received the Bachelors of Technology degree in Electrical Engineering from Government Engineering College, Guru Gasidas University, Bilaspur, Chhattisgarh, India in 2007, and pursuing Masters of Engineering in Instrumentation and Control Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India. His current research and teaching interests are in Control and Power system. He has authored more than 4 research publications.